

ZZZ8
DAZ@
DAZ04300100
PCB

ZZZ1
DA2@
MAIN BOARD
DA600007E10
PCB

ZZZ2
DA2@
E board
DA40000A910
PCB

ZZZ3
DA2@
FP board
DA600007D10
PCB

ZZZ4
DA2@
Function board
DA40000AA10
PCB

ZZZ5
DA2@
USB board
DA40000AB10
PCB

ZZZ6
DA2@
IO board
DA40000AC10
PCB

ZZZ7
DA2@
Power board
DA40000AD10
PCB

Compal Confidential

KAQB0 M/B Schematics Document

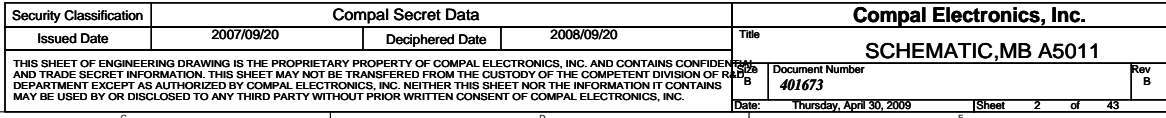
Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2009-03-27

REV:1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2007/09/29	Deciphered Date	2007/09/29	Title	SCHEMATIC,MB A5011
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Model Name : KAQB0
File Name : LA5011P
P/N:DA60000B110



power plane State	+B	+5VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE
		+3VALW		+1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

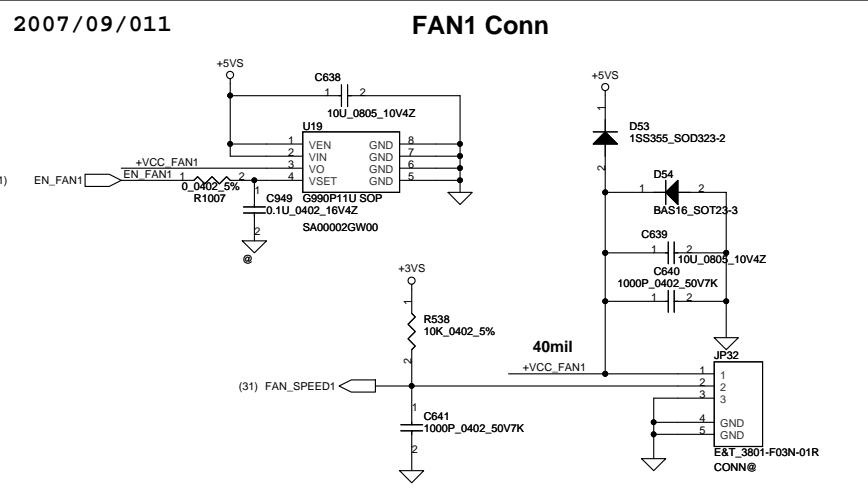
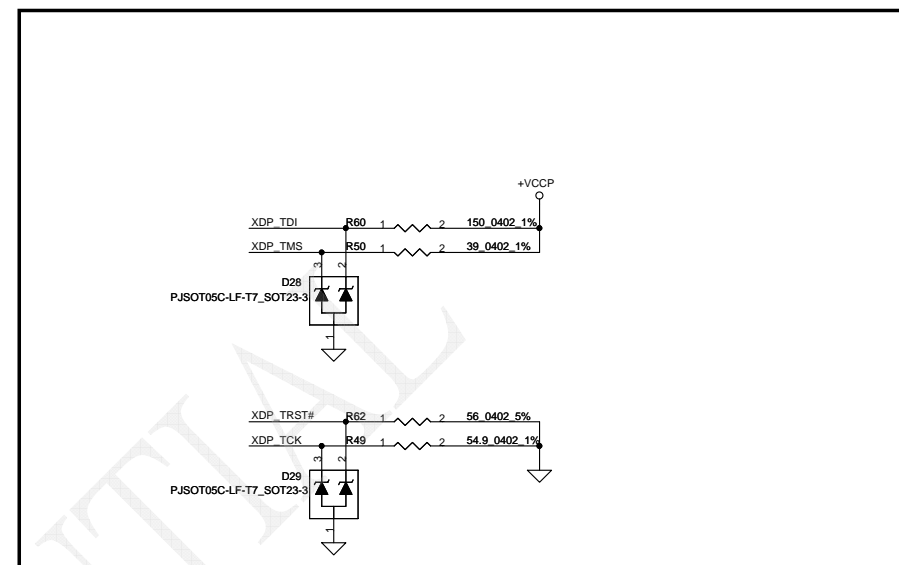
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

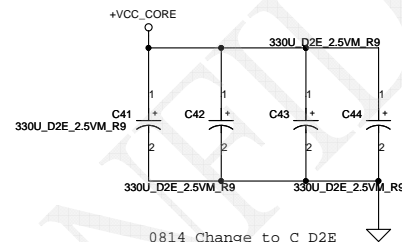
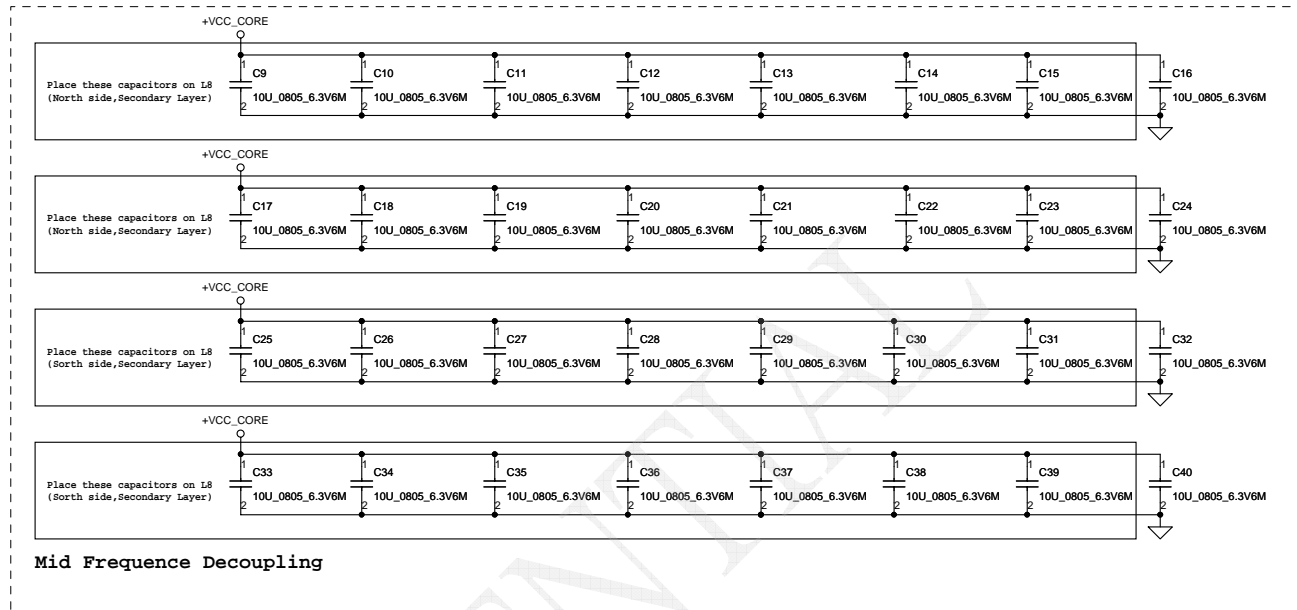
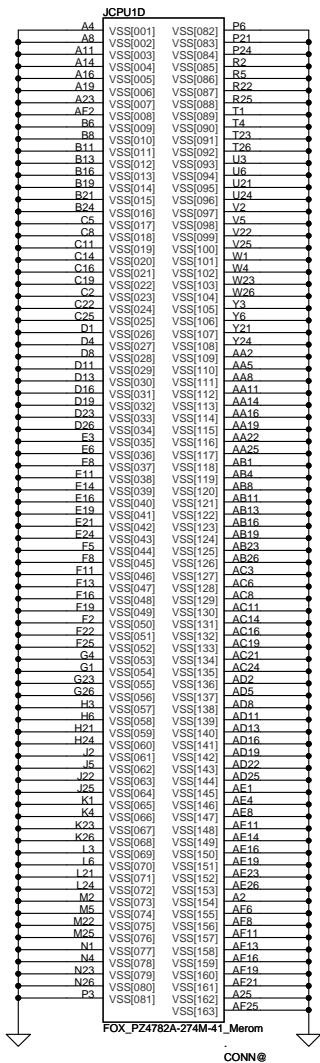
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

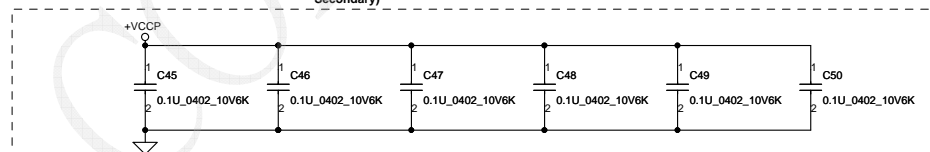
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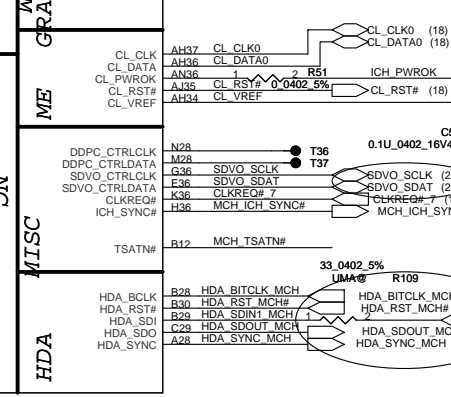
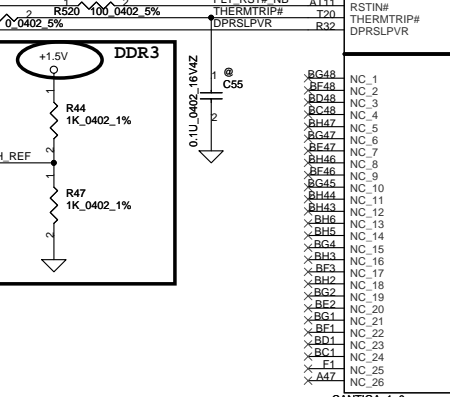
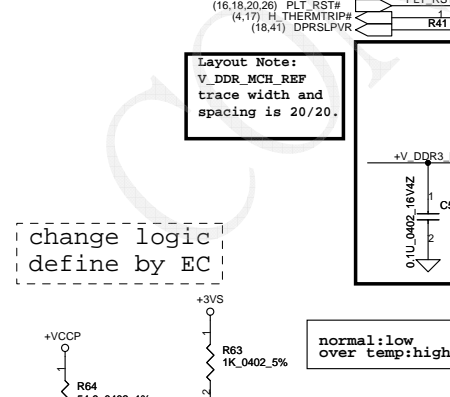
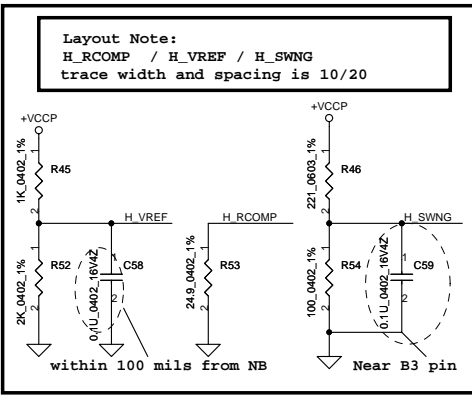
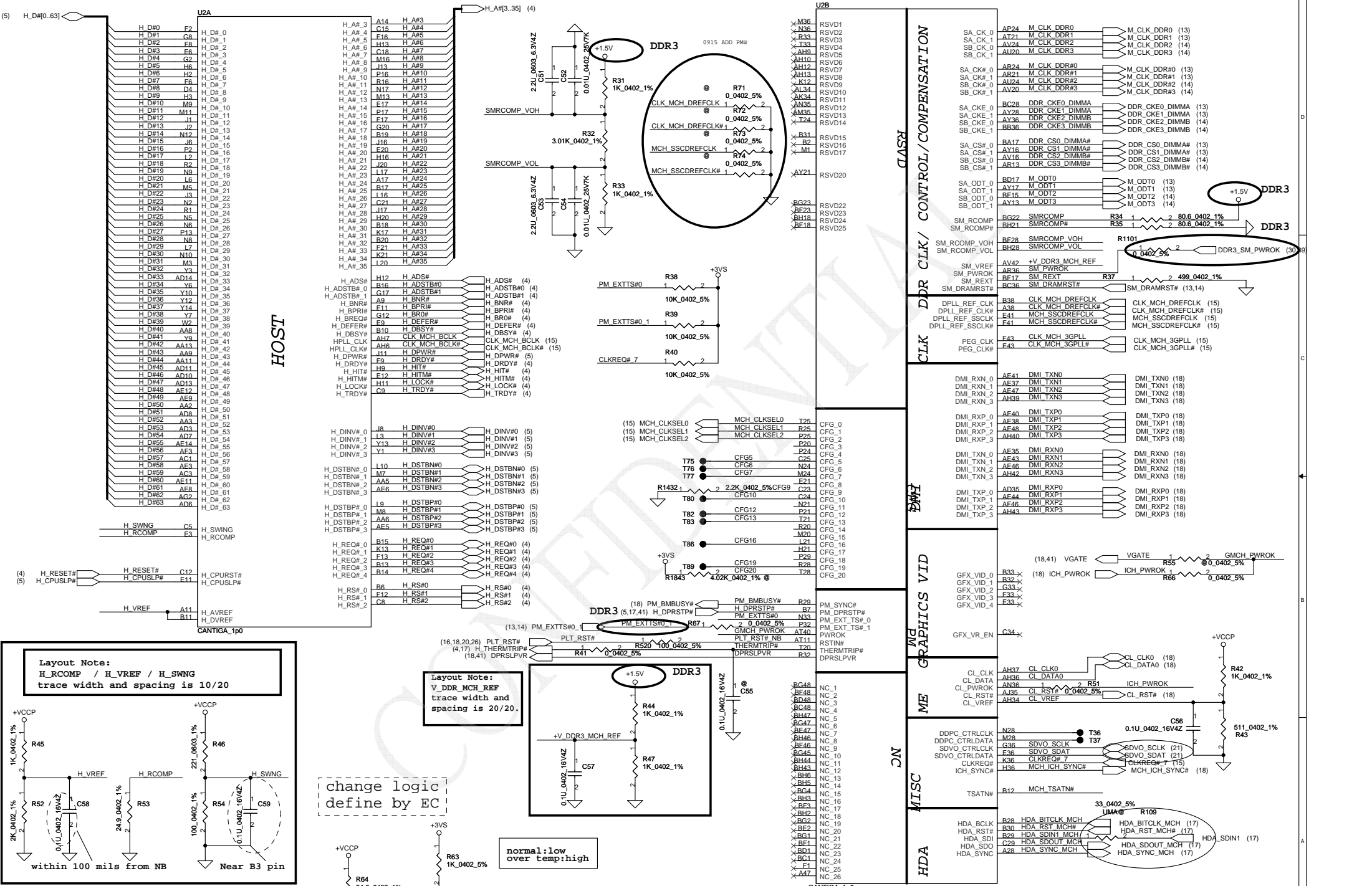
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Place these inside socket cavity on L8 (North side Secondary)

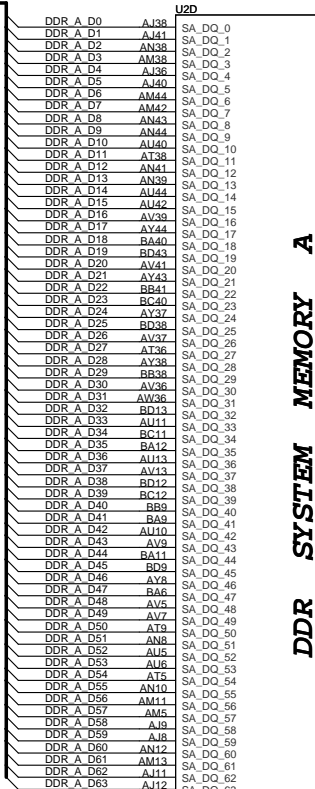


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(13) DDR_A_D[0..63]



DDR SYSTEM MEMORY A

CANTIGA_1p0

SA_BS_0 BD21 DDR A BS0
SA_BS_1 BG18 DDR A BS1
SA_BS_2 AT25 DDR A BS2

SA_RAS# BB20 DDR A RAS#
SA_CAS# BD20 DDR A CAS#
SA_WE# AY20 DDR A WE#

DDR_A_DM[0..7] (13)
AM37 DDR A DM0
AT41 DDR A DM1
AY41 DDR A DM2
AU39 DDR A DM3
BB12 DDR A DM4
AY6 DDR A DM5
AT7 DDR A DM6
AJ5 DDR A DM7

DDR_A_DQS[0..7] (13)

SA_DQS_0 AJ44 DDR A DQS0
SA_DQS_1 AT44 DDR A DQS1
SA_DQS_2 BA43 DDR A DQS2
SA_DQS_3 RC37 DDR A DQS3
SA_DQS_4 AW12 DDR A DQS4
SA_DQS_5 BC8 DDR A DQS5
SA_DQS_6 AU8 DDR A DQS6
SA_DQS_7 AM7 DDR A DQS7

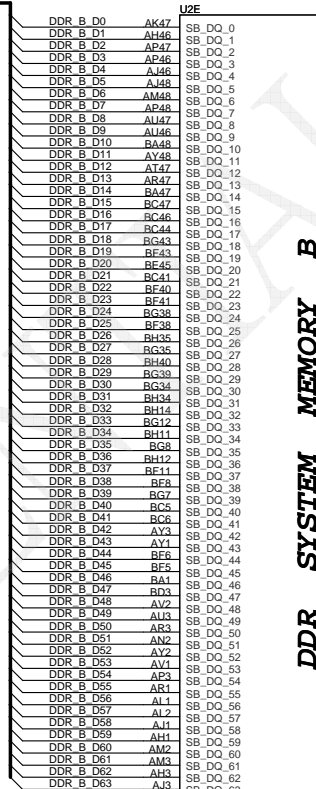
DDR_A_DQS#0[0..7] (13)

SA_DQS#_0 AJ43 DDR A DQS#0
SA_DQS#_1 AT43 DDR A DQS#1
SA_DQS#_2 BA44 DDR A DQS#2
SA_DQS#_3 BD37 DDR A DQS#3
SA_DQS#_4 AY12 DDR A DQS#4
SA_DQS#_5 BD8 DDR A DQS#5
SA_DQS#_6 AU9 DDR A DQS#6
SA_DQS#_7 AM8 DDR A DQS#7

DDR_A_MA[0..14] (13)

BA21 DDR A MA0
BC24 DDR A MA1
BG24 DDR A MA2
BH24 DDR A MA3
BC25 DDR A MA4
BA24 DDR A MA5
BD24 DDR A MA6
BF25 DDR A MA7
AW24 DDR A MA9
BC21 DDR A MA10
BG26 DDR A MA11
BH26 DDR A MA12
BH17 DDR A MA13
AY25 DDR A MA14

(14) DDR_B_D[0..63]



DDR SYSTEM MEMORY B

CANTIGA_1p0

SB_BS_0 BC16 DDR B BS0
SB_BS_1 BB17 DDR B BS1
SB_BS_2 BB33 DDR B BS2

SB_RAS# AU17 DDR B RAS#
SB_CAS# BC16 DDR B CAS#
SB_WE# BF14 DDR B WE#

DDR_B_DM[0..7] (14)
AM47 DDR B DM0
AY47 DDR B DM1
BD40 DDR B DM2
BF45 DDR B DM3
BC11 DDR B DM4
BA3 DDR B DM5
AP1 DDR B DM6
AK2 DDR B DM7

DDR_B_DQS[0..7] (14)

SB_DQS_0 AL47 DDR B DQS0
SB_DQS_1 AV48 DDR B DQS1
SB_DQS_2 BC41 DDR B DQS2
SB_DQS_3 BC37 DDR B DQS3
SB_DQS_4 BH9 DDR B DQS4
SB_DQS_5 BB2 DDR B DQS5
SB_DQS_6 AU11 DDR B DQS6
SB_DQS_7 AM6 DDR B DQS7

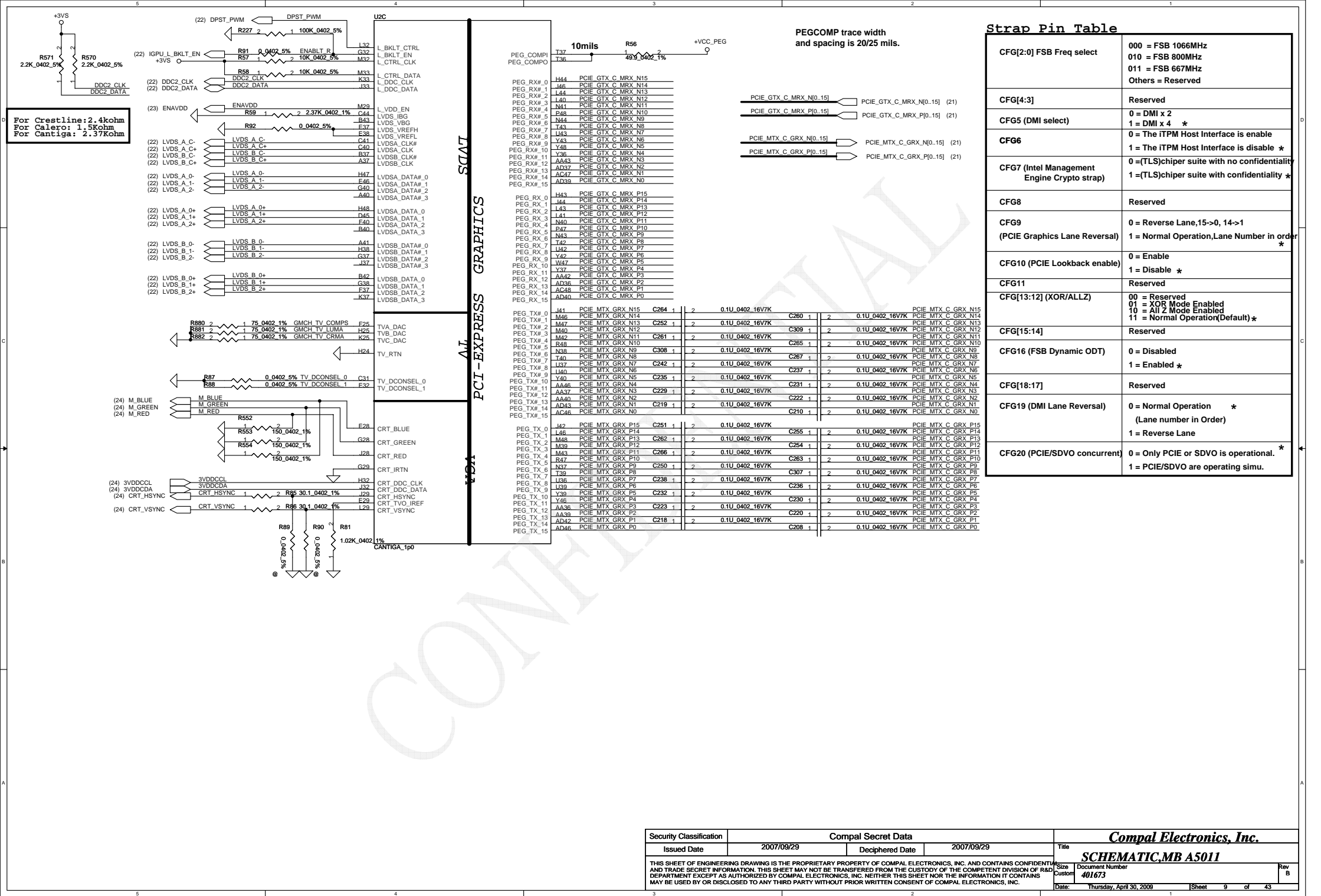
DDR_B_DQS#0[0..7] (14)

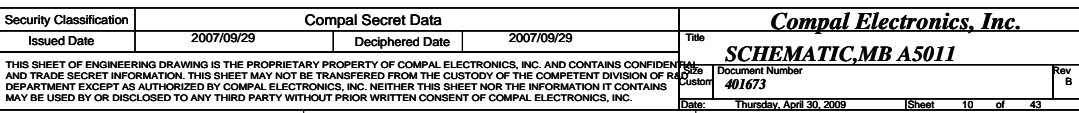
SB_DQS#_0 AL46 DDR B DQS#0
SB_DQS#_1 AV47 DDR B DQS#1
SB_DQS#_2 BH41 DDR B DQS#2
SB_DQS#_3 BH37 DDR B DQS#3
SB_DQS#_4 BG9 DDR B DQS#4
SB_DQS#_5 BC2 DDR B DQS#5
SB_DQS#_6 AT2 DDR B DQS#6
SB_DQS#_7 AN5 DDR B DQS#7

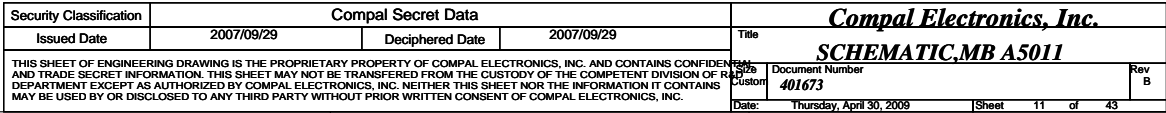
DDR_B_MA[0..14] (14)

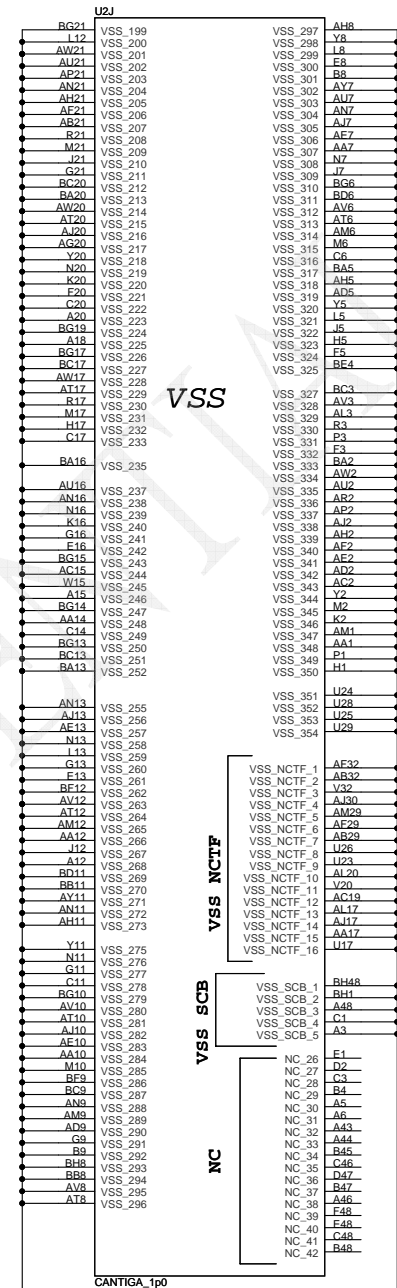
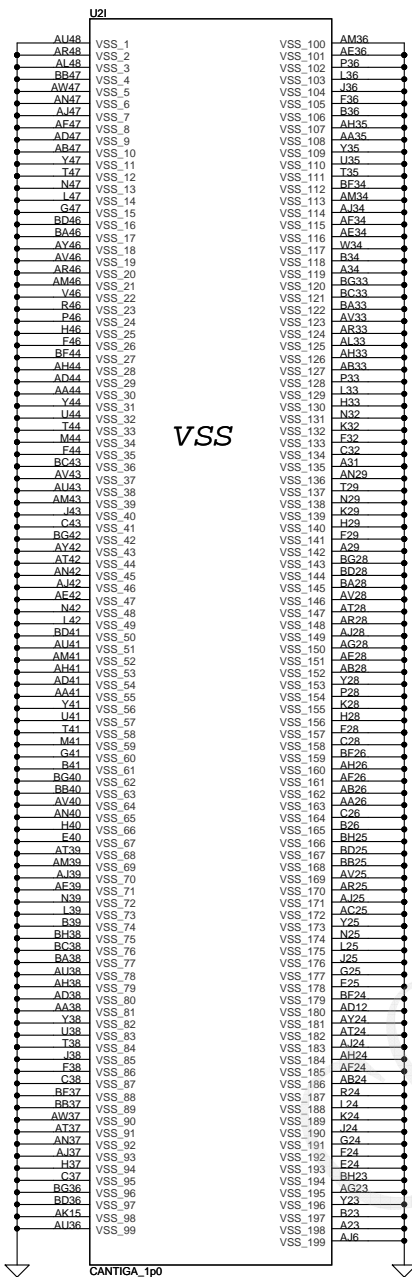
AV17 DDR B MA0
BA25 DDR B MA1
RC25 DDR B MA2
AU25 DDR B MA3
AW25 DDR B MA4
BB28 DDR B MA5
AU28 DDR B MA6
AW28 DDR B MA7
AT33 DDR B MA8
BD33 DDR B MA9
BB16 DDR B MA10
AW33 DDR B MA11
BH15 DDR B MA12
AU33 DDR B MA14

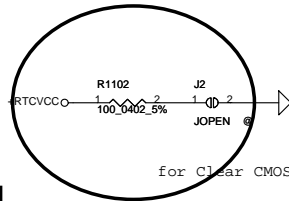
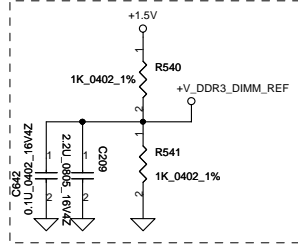
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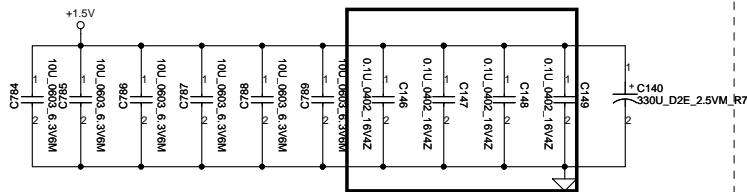




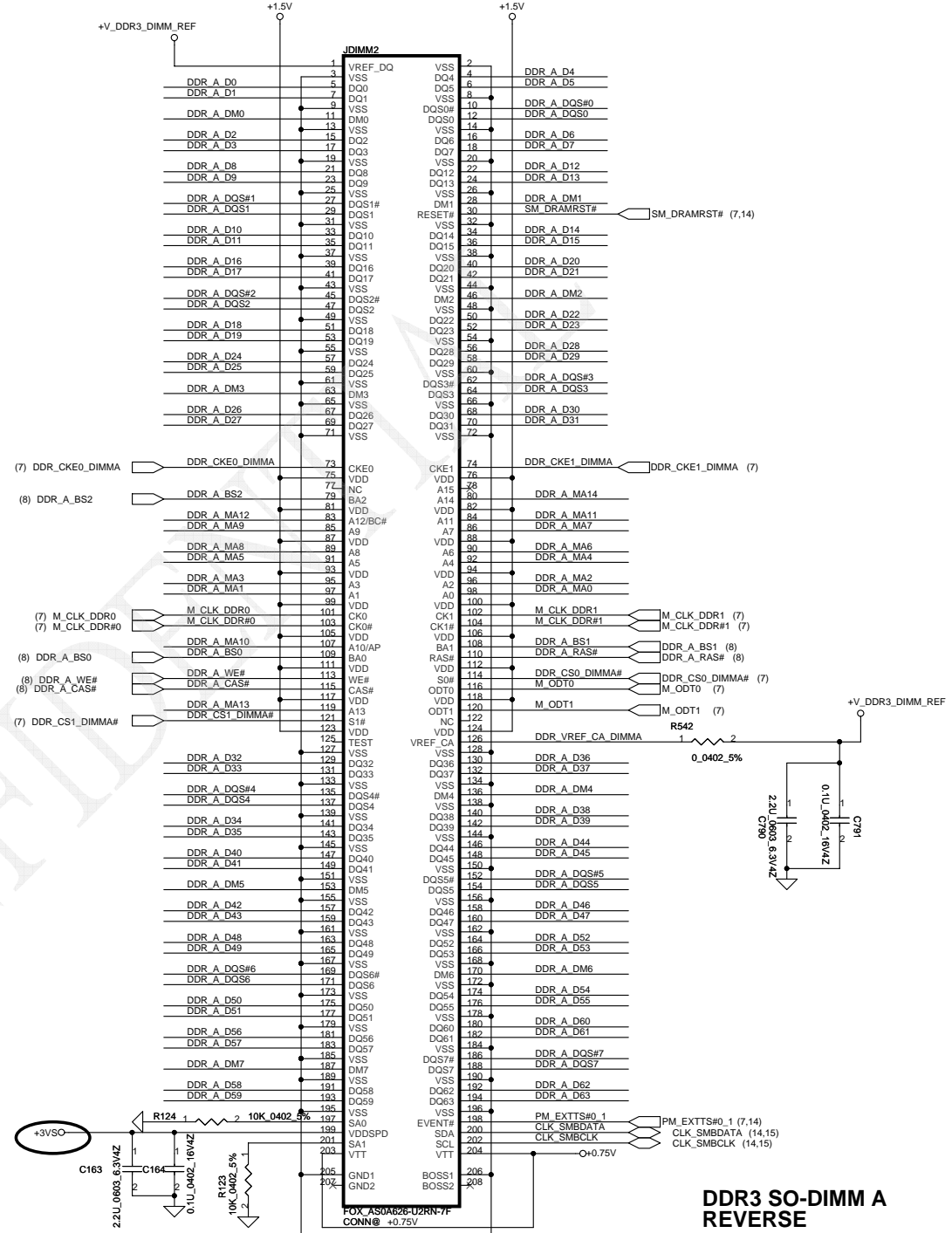
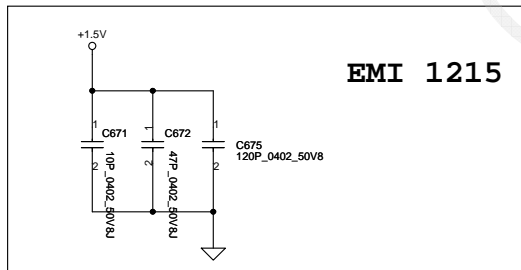
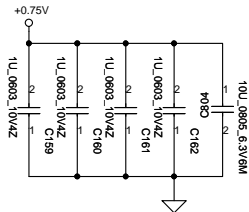


Layout Note:
Place near JP4

Layout Note: Place these 4 Caps near Command
and Control-signals-of-DIMMA



Layout Note:
Place near JP4.203 & JP4.204



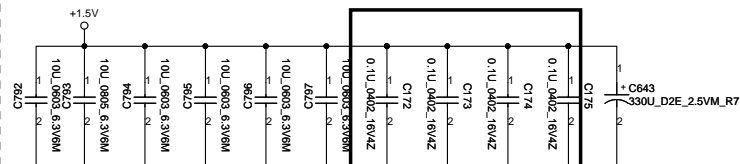
DDR3 SO-DIMM A
REVERSE

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- (8) DDR_B_DQS#[0..7]
- (8) DDR_B_DQ[0..63]
- (8) DDR_B_DM[0..7]
- (8) DDR_B_DQS[0..7]
- (8) DDR_B_MA[0..14]

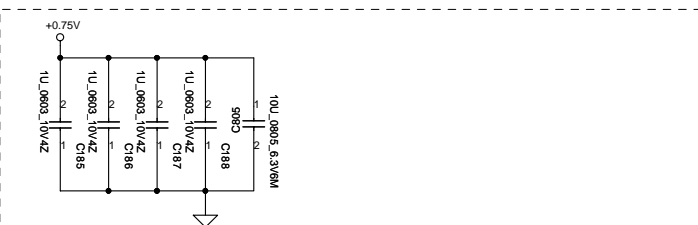
Layout Note:
Place near JP5

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA

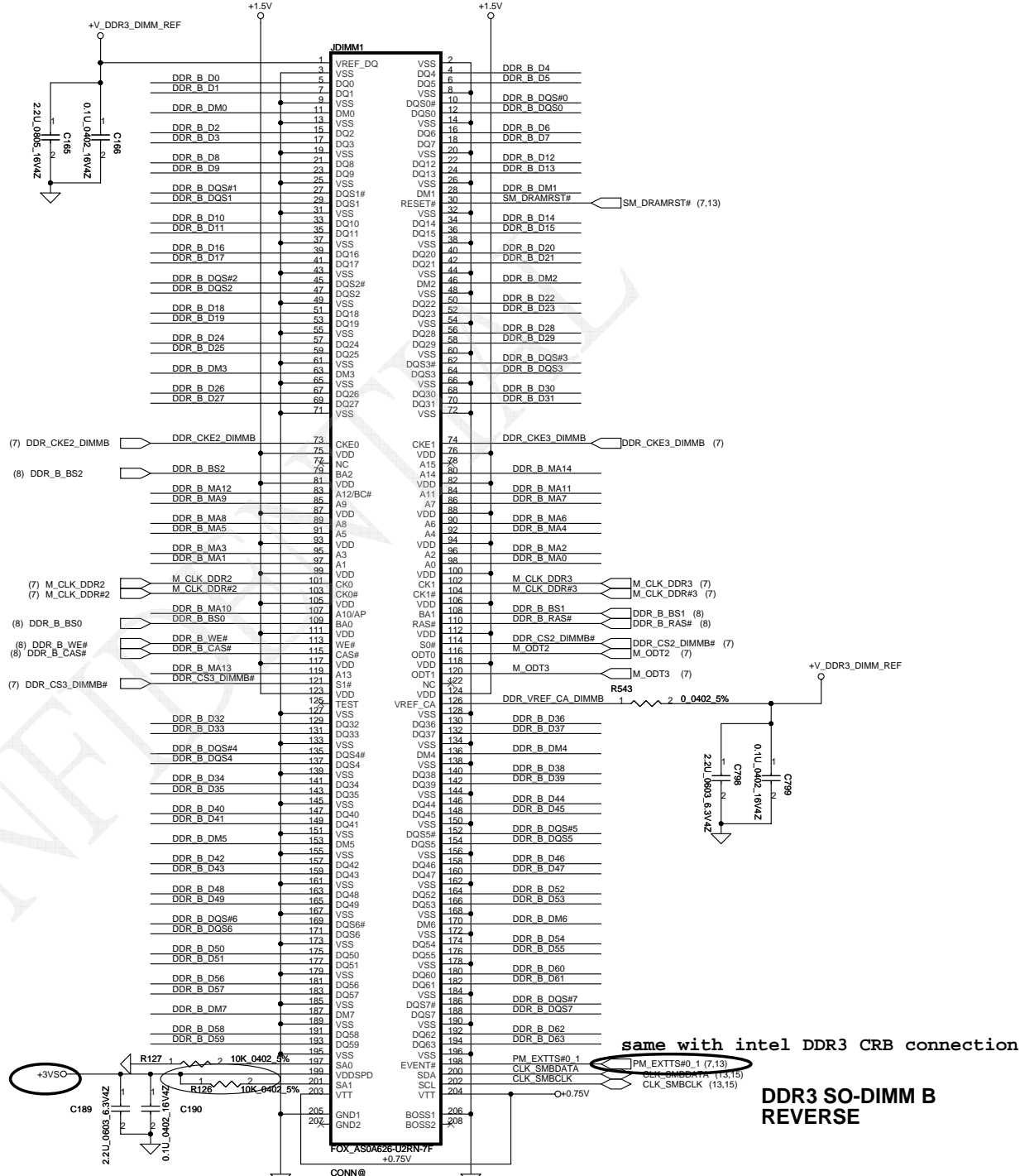
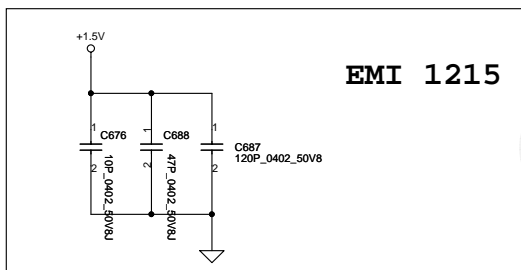


Layout Note:
Place near JP5.203 & JP5.204

<BOM Structure>



EMI 1215



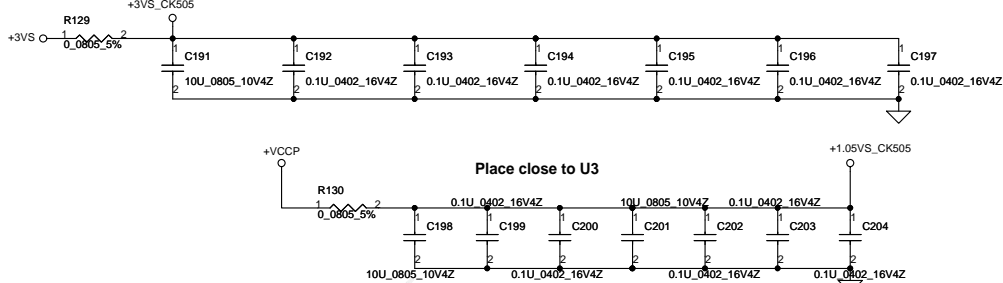
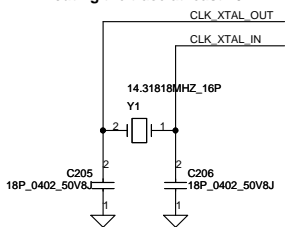
same with intel DDR3 CRB connection

DDR3 SO-DIMM B
REVERSE

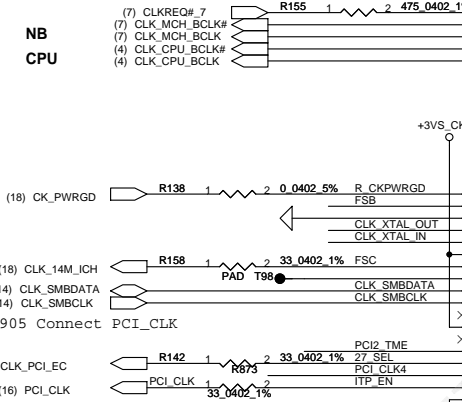
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FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

Routing the trace at least 10mil

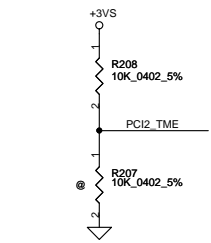
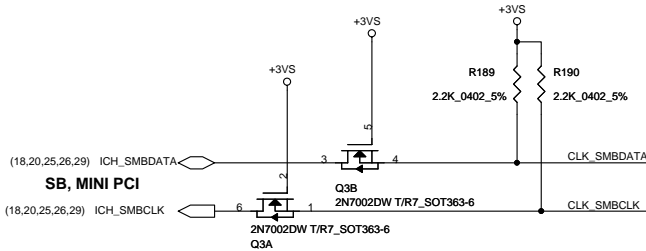
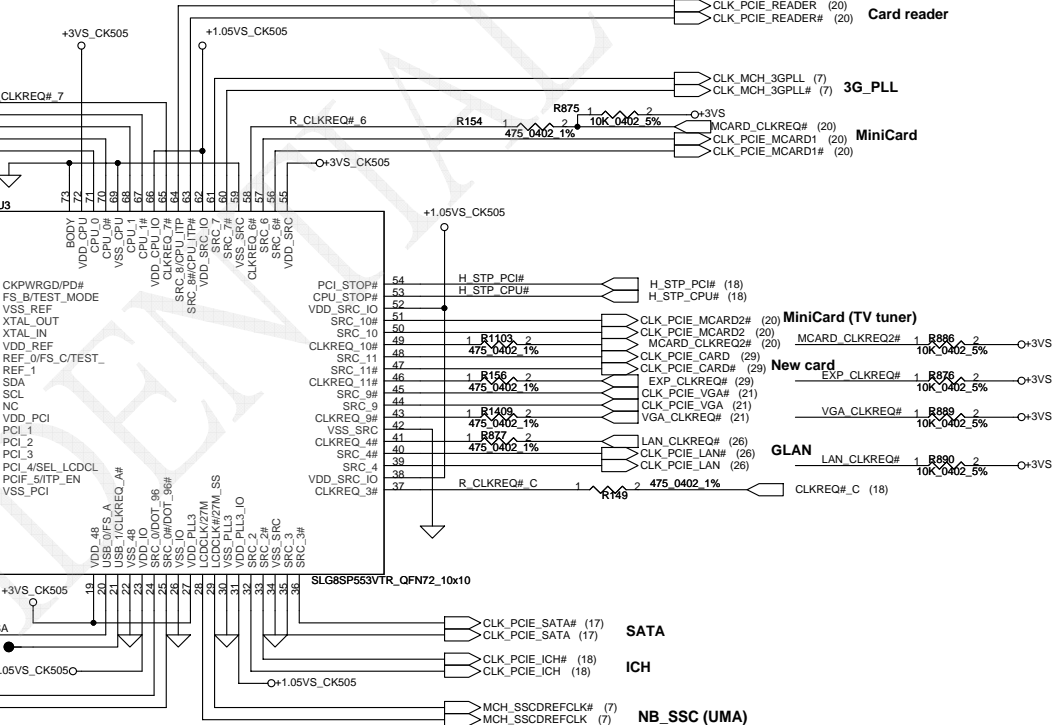
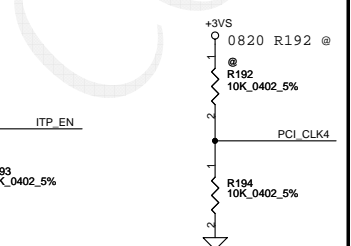


NB CPU



NB (UMA)

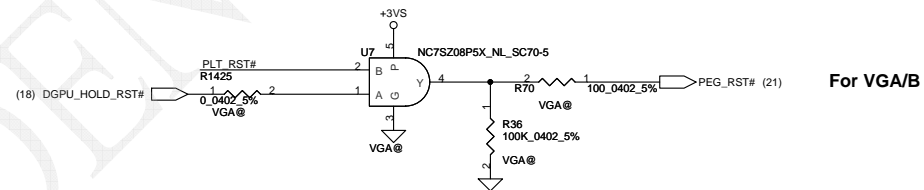
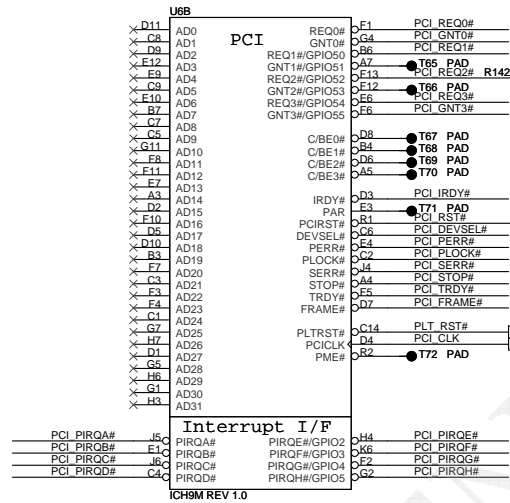
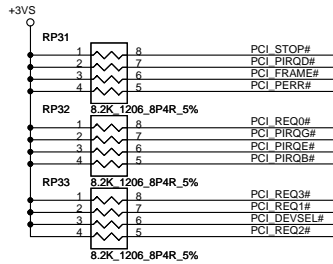
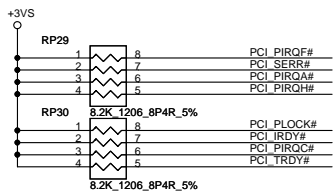
ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
PCI_CLK3	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)



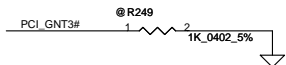
for ICS Overclocking setting
0=Overclocking of CPU and SRC allowed
1=Overclocking of CPU and SRC NOT allowed

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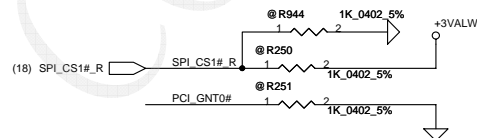
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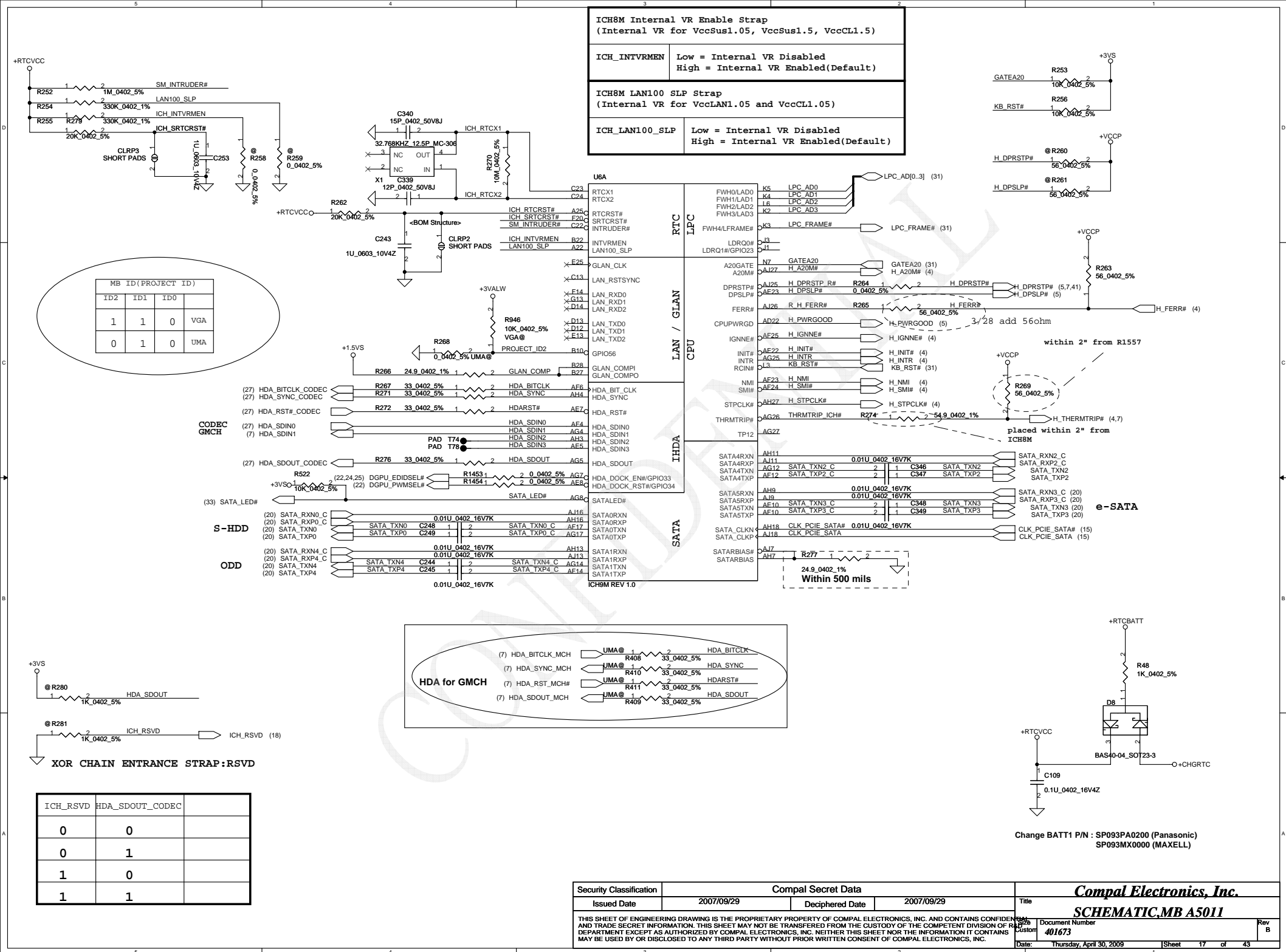


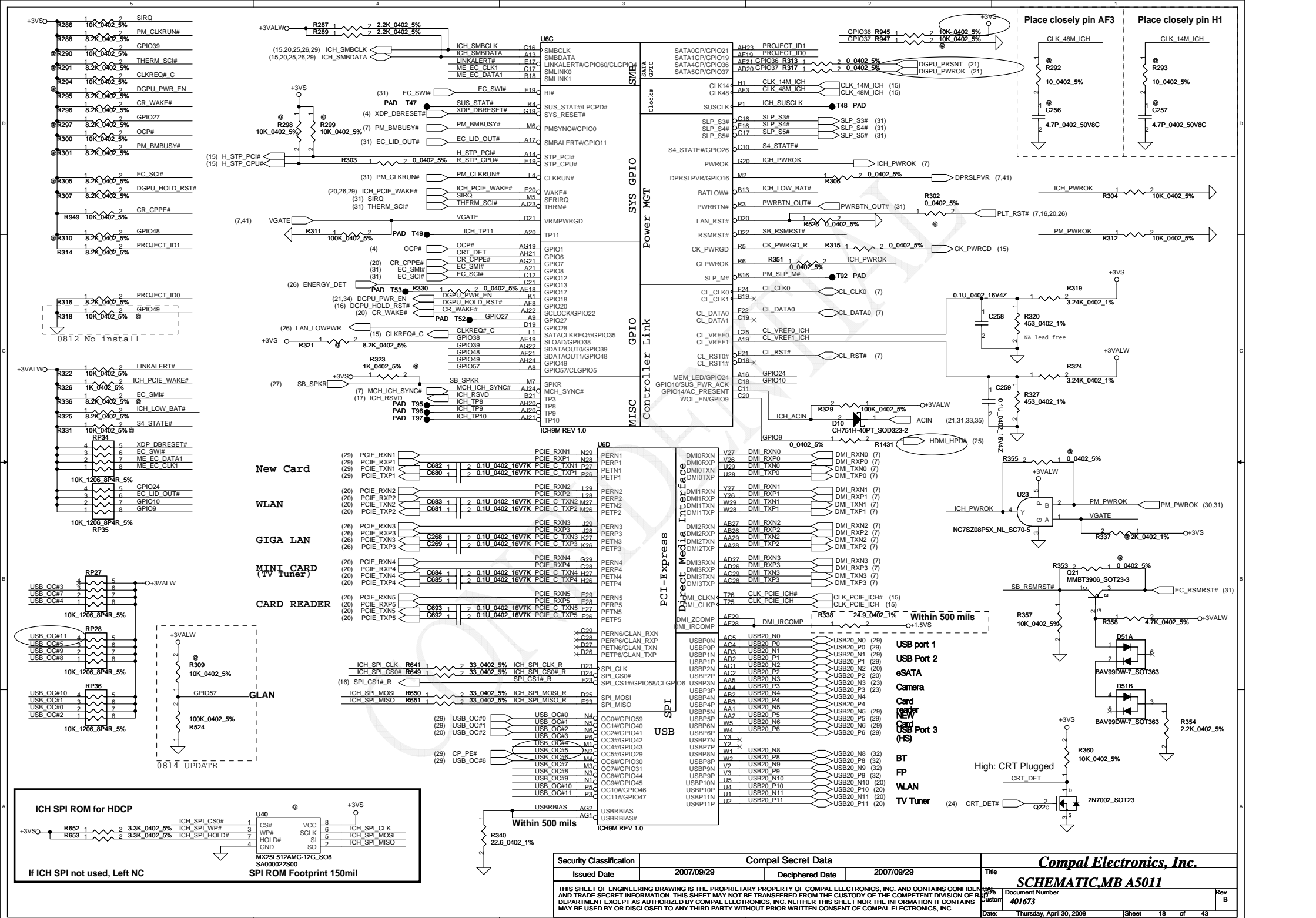
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



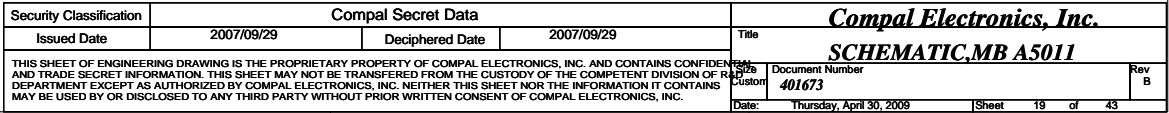
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

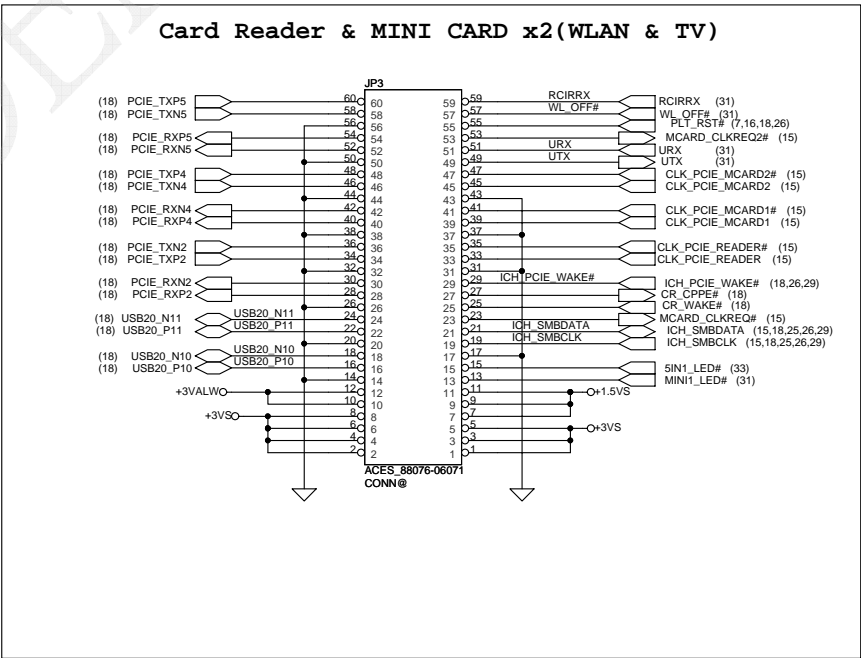
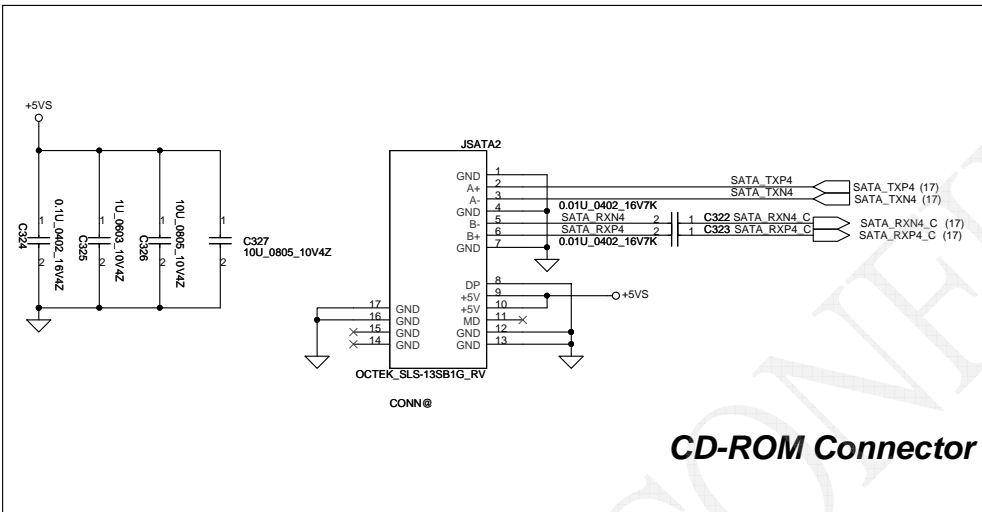
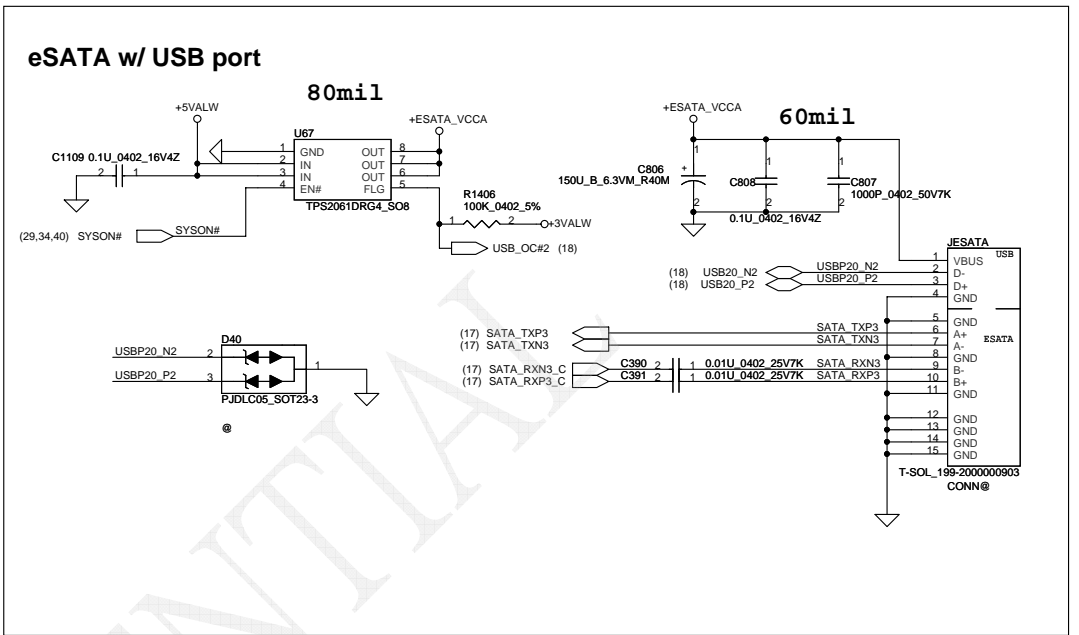
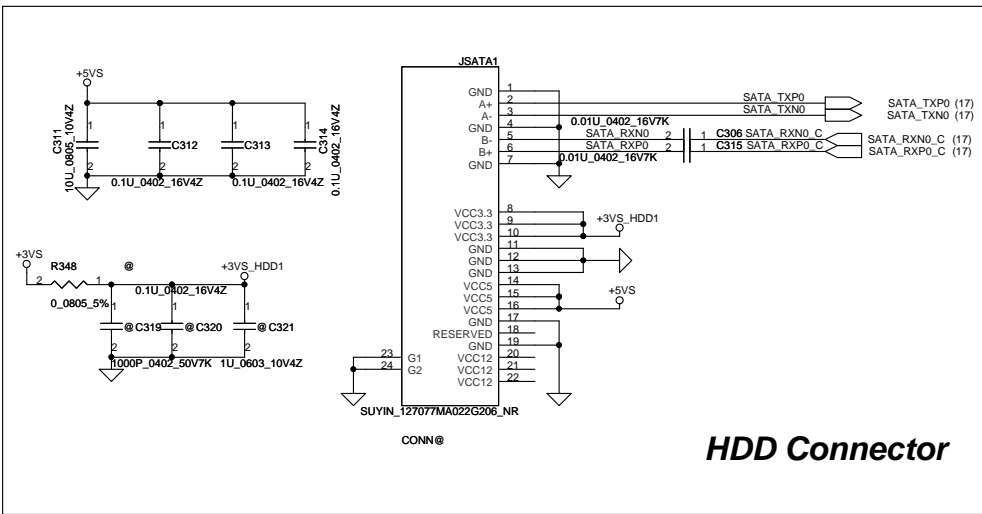




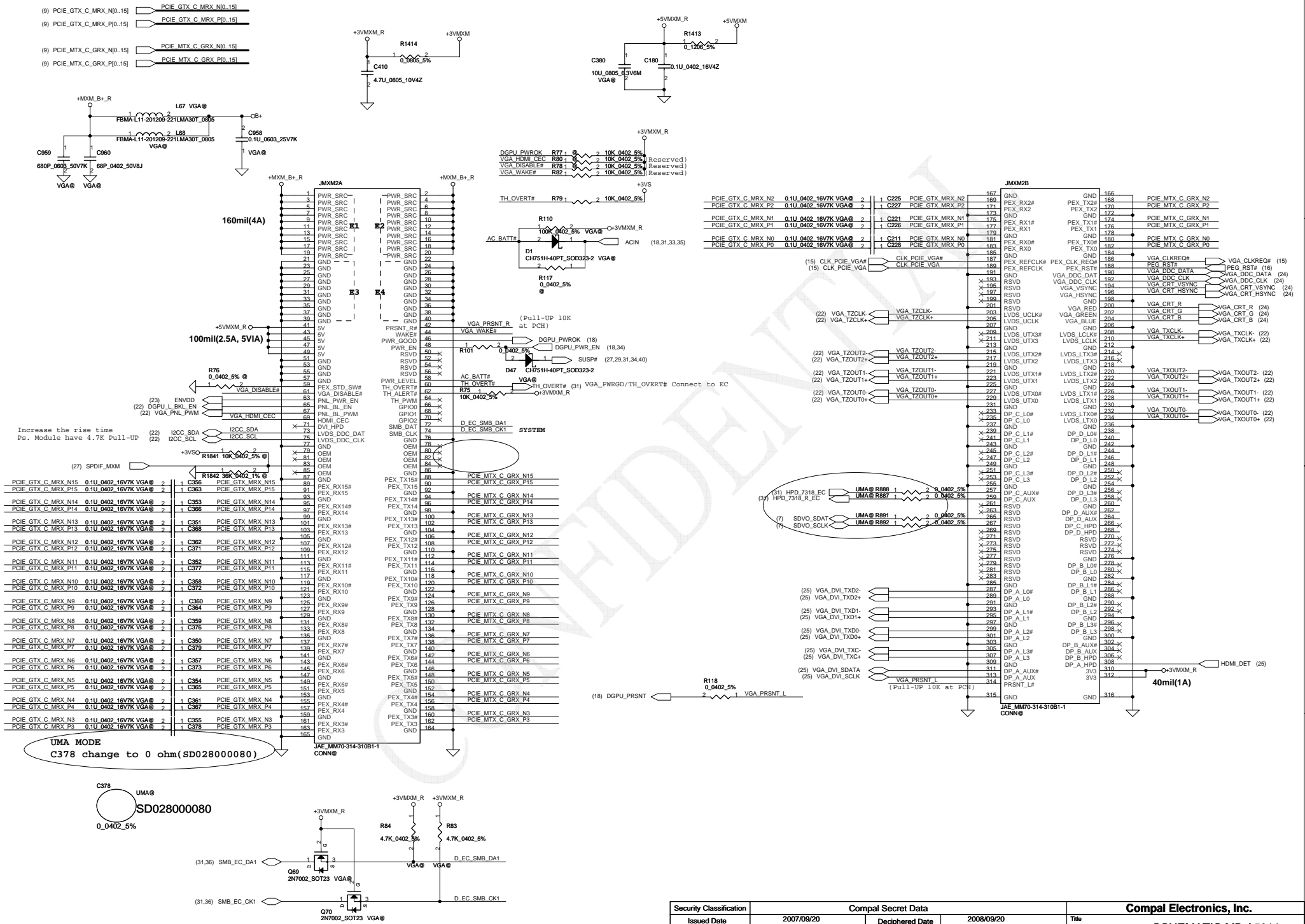


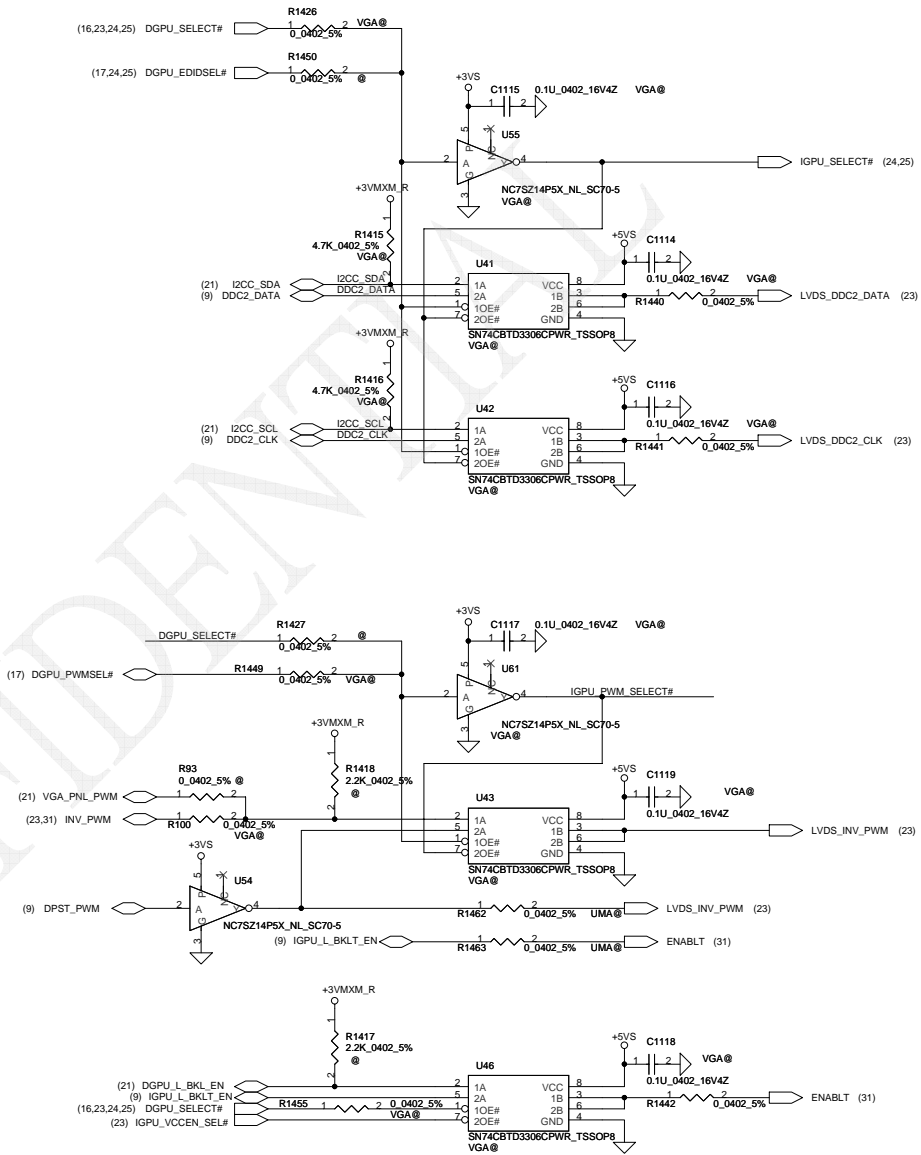
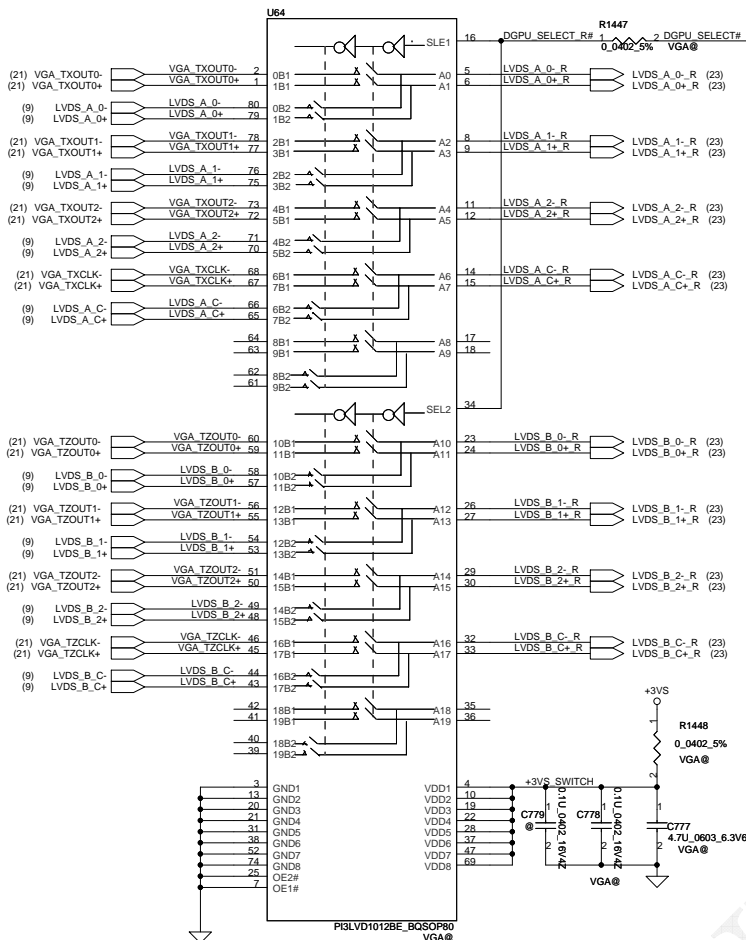
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				Rev. B	
				Rev. C	
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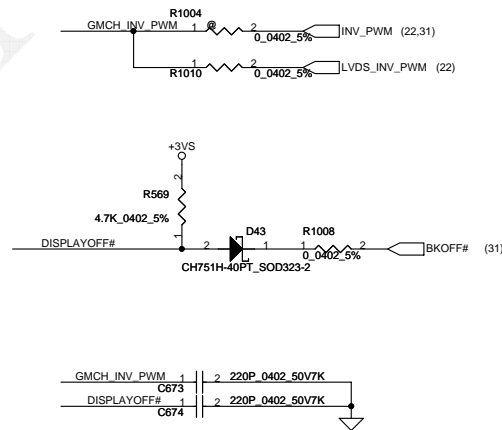
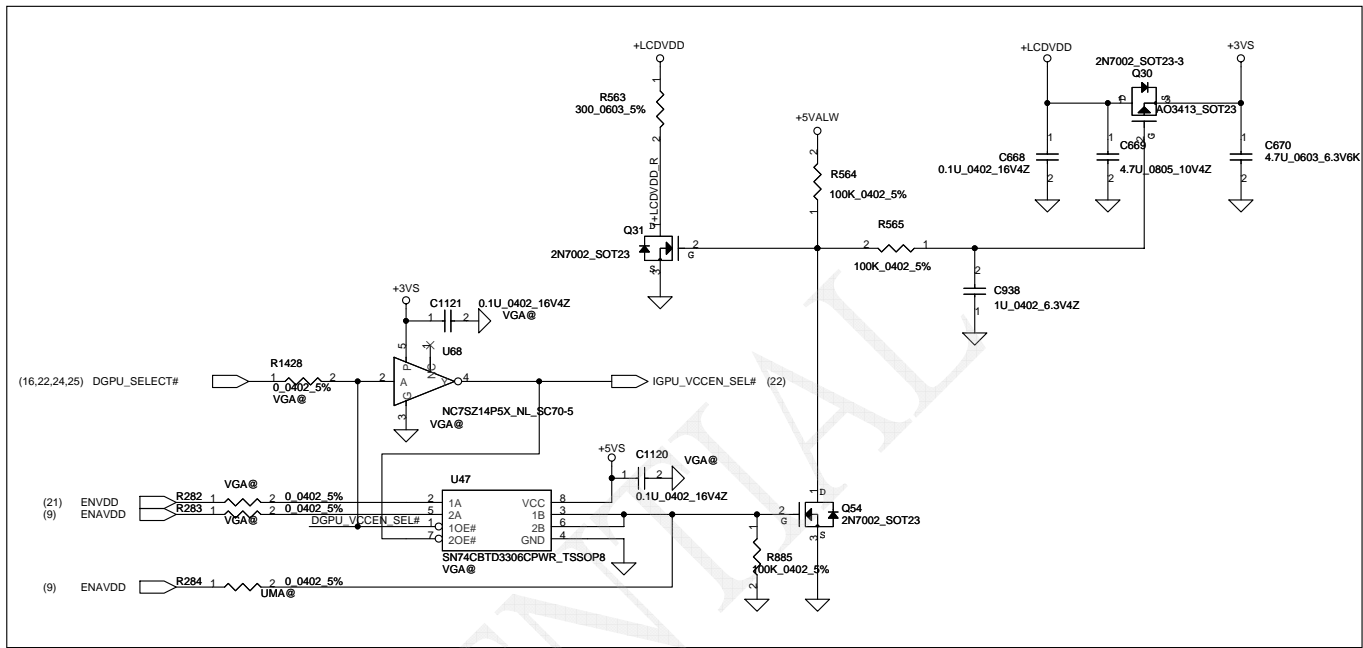
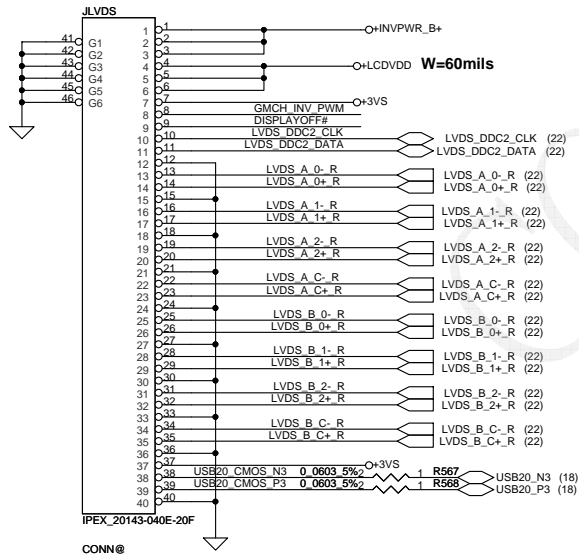
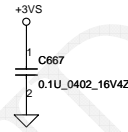
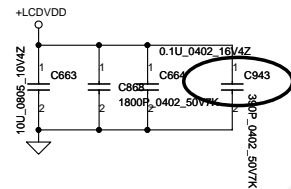
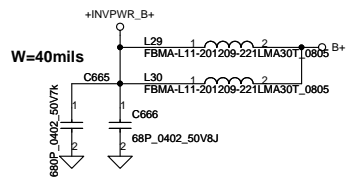
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Issued Date	2007/09/29	Deciphered Date	2007/09/29	Document Number	401673	Rev	B
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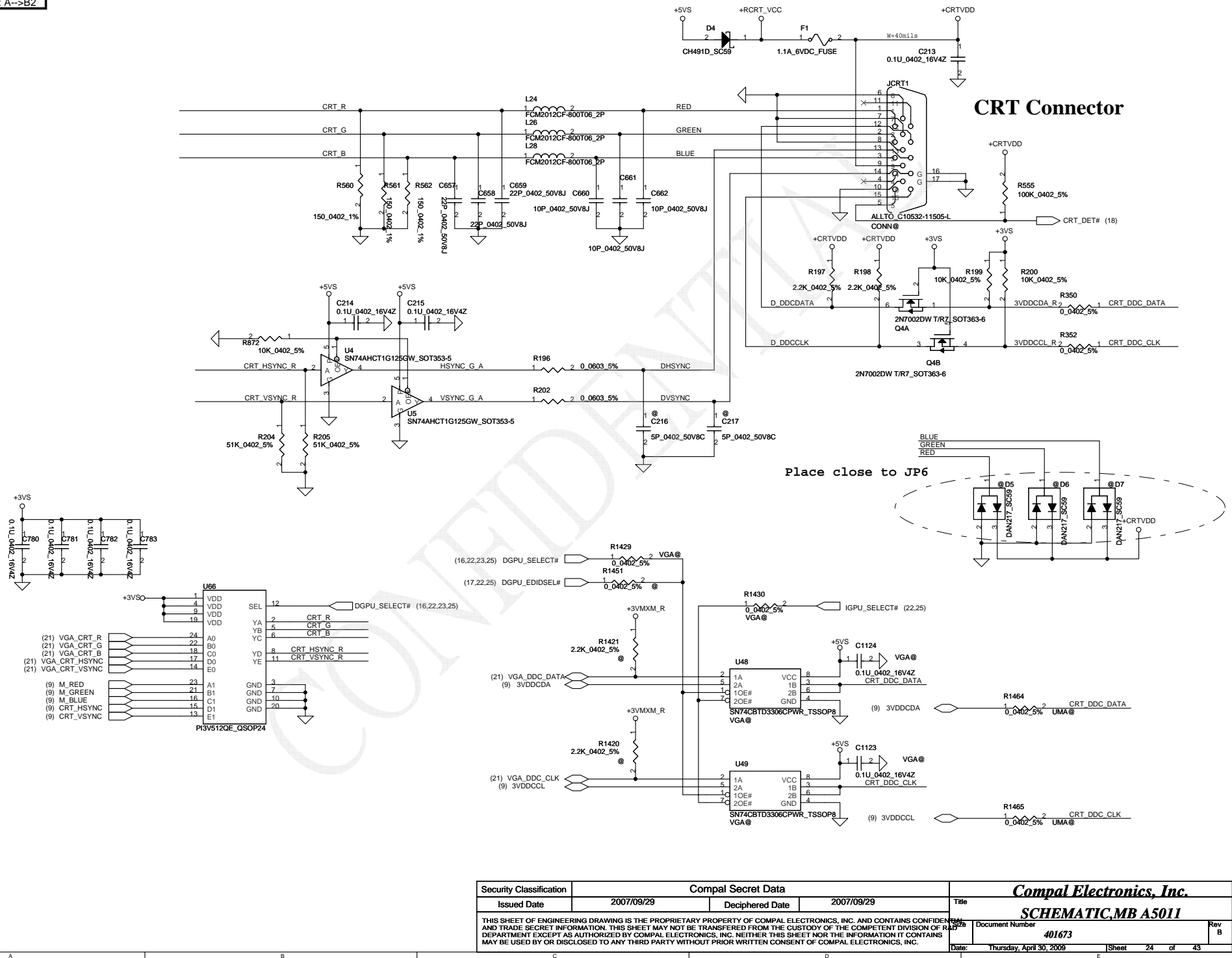
LVDS and USB CAM connector



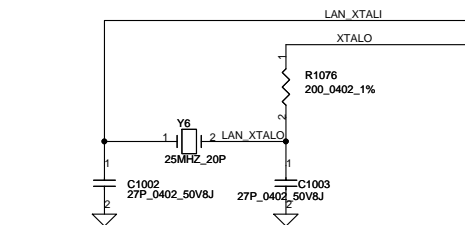
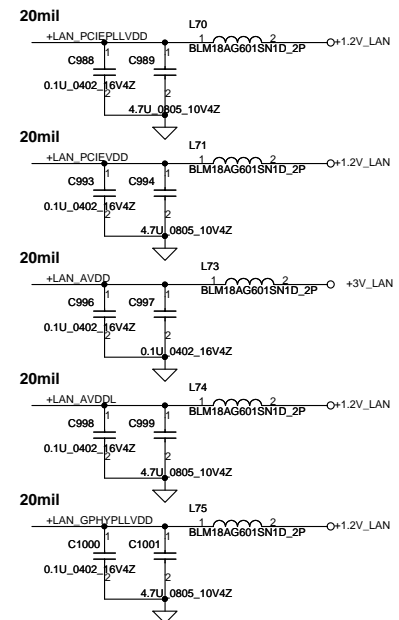
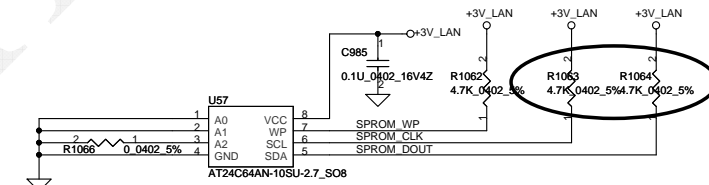
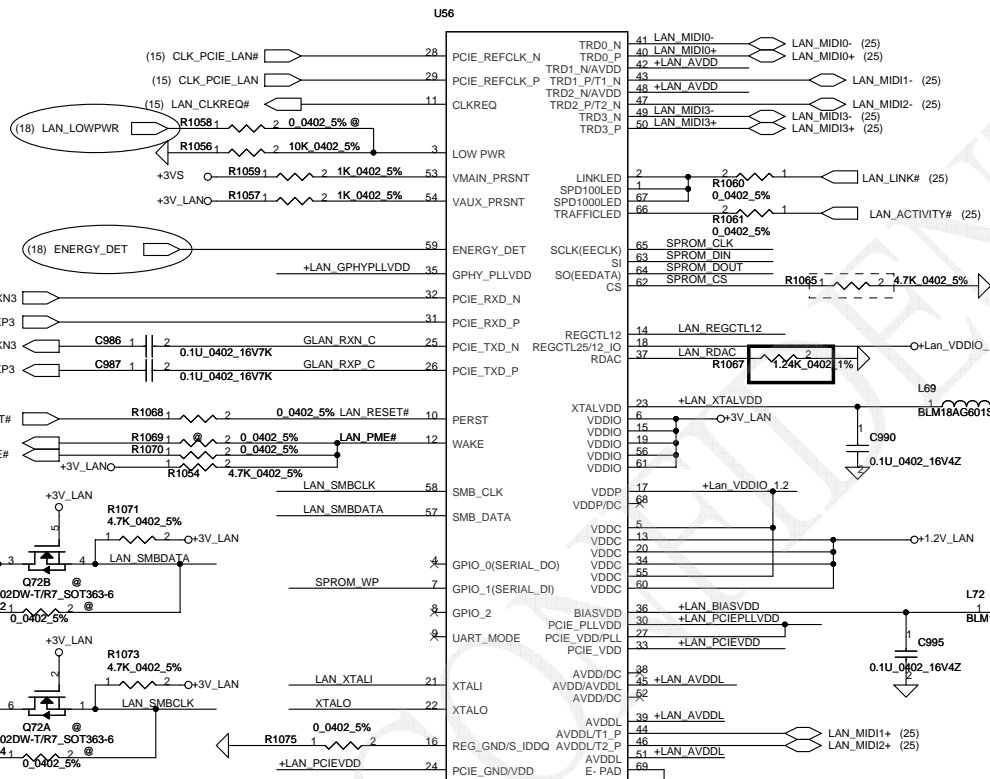
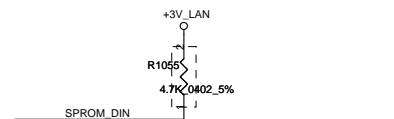
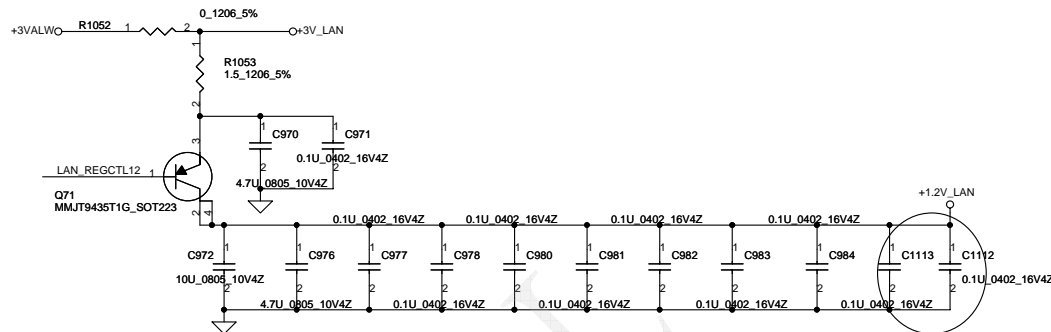
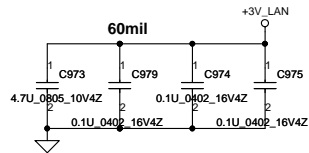
Security Classification		Compal Secret Data		Title	
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Compal Electronics, Inc.
SCHEMATIC_MB A5011

NOTE: L: A-->B1
H: A-->B2



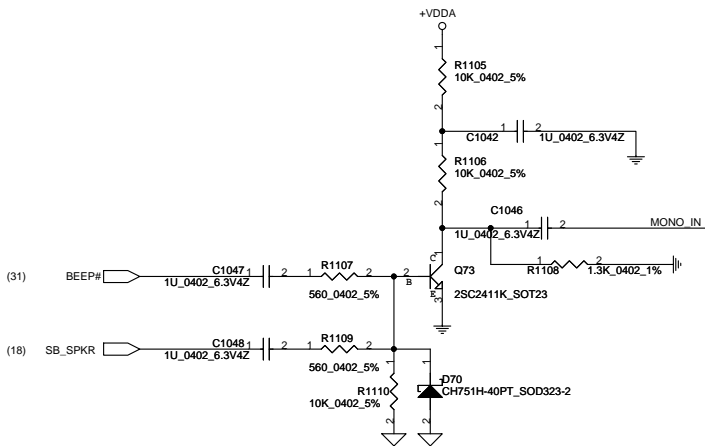
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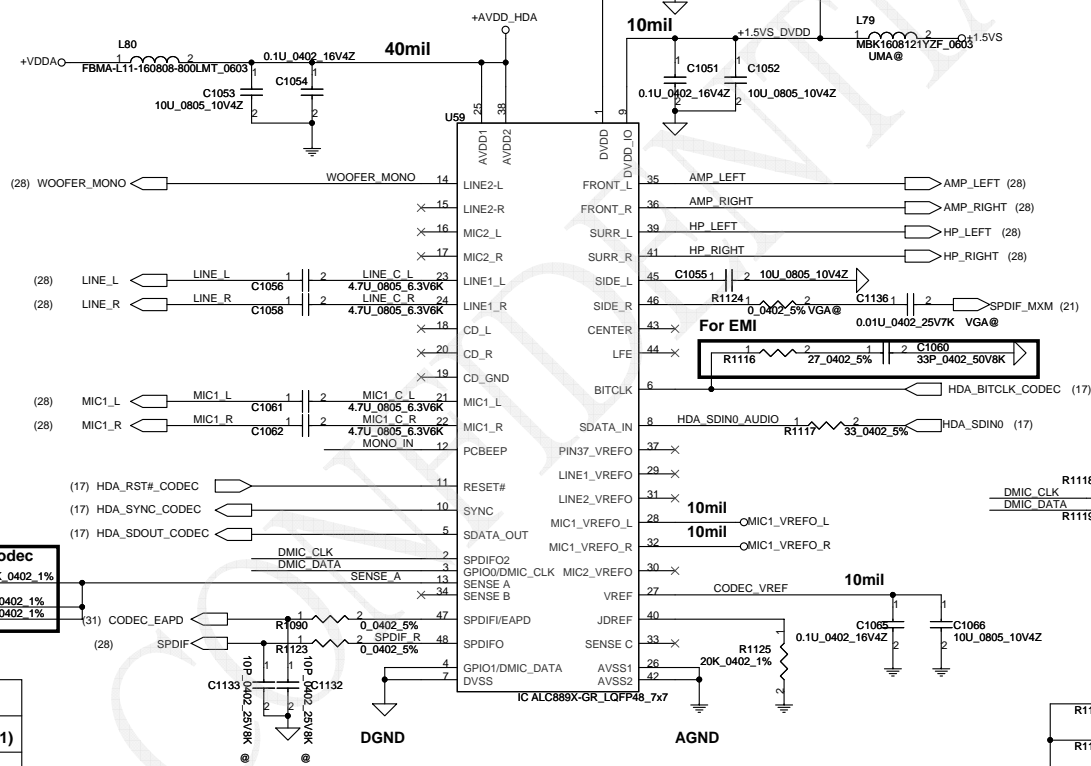
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Place closed to Pin2 & Pin59

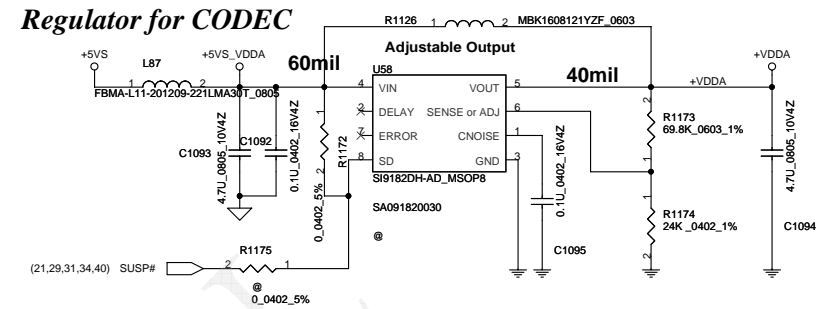
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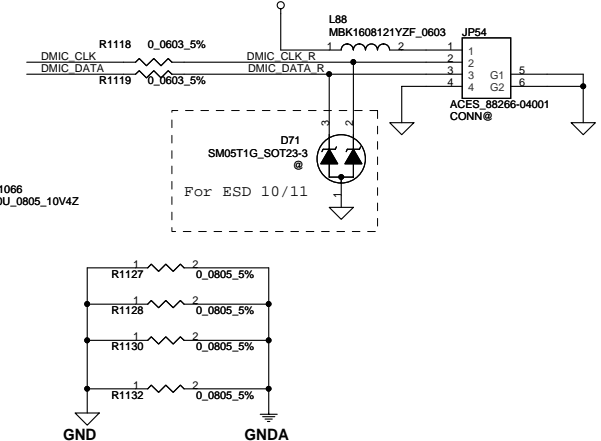
HD Audio Codec



Regulator for CODEC

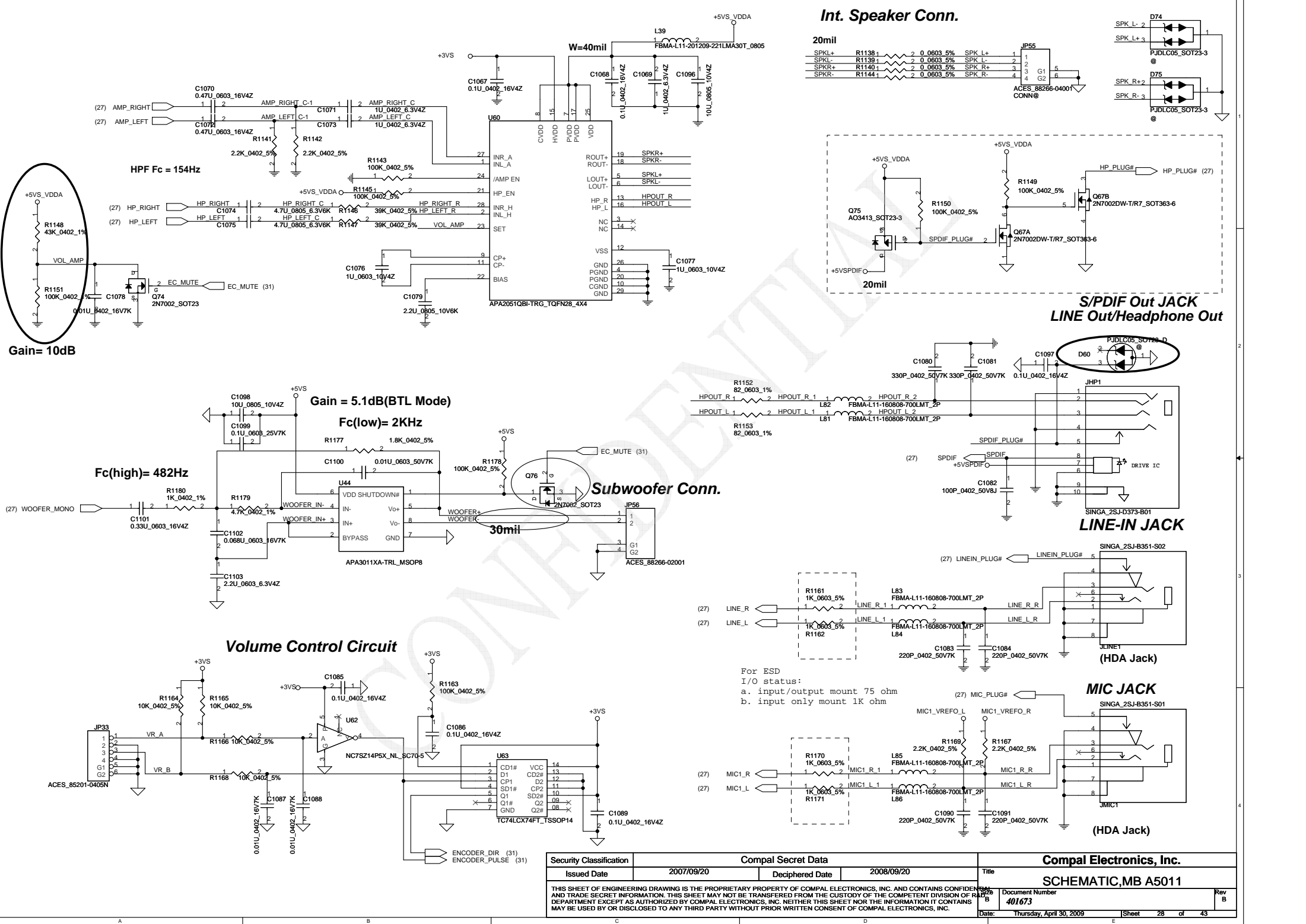


Digital MIC



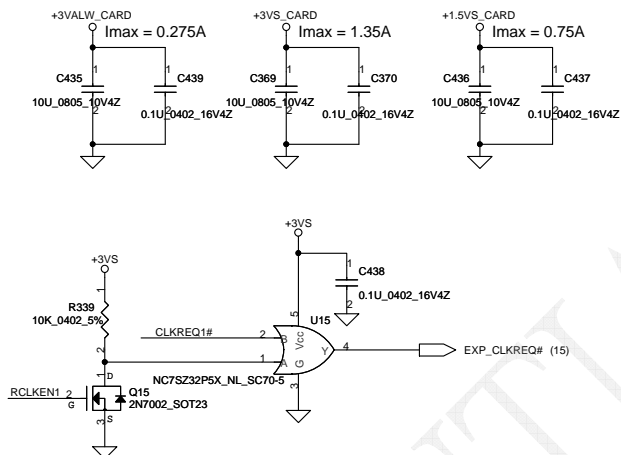
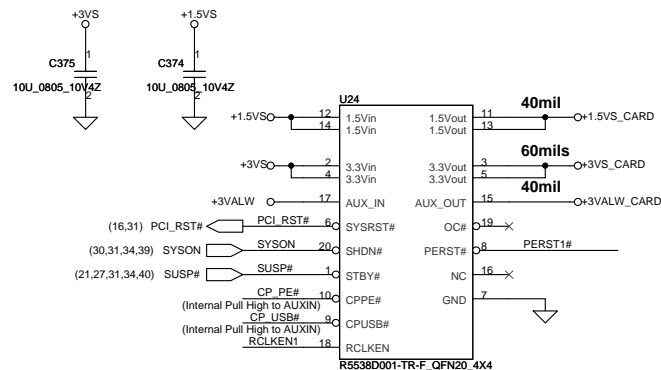
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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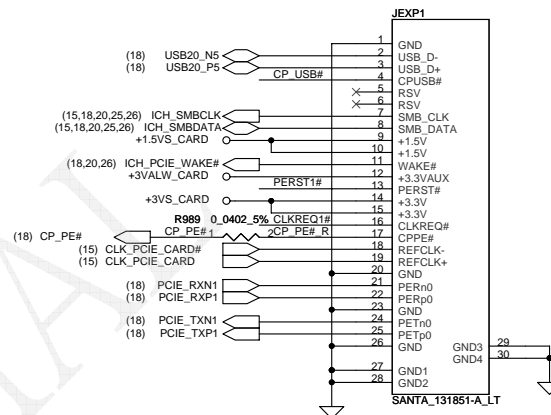


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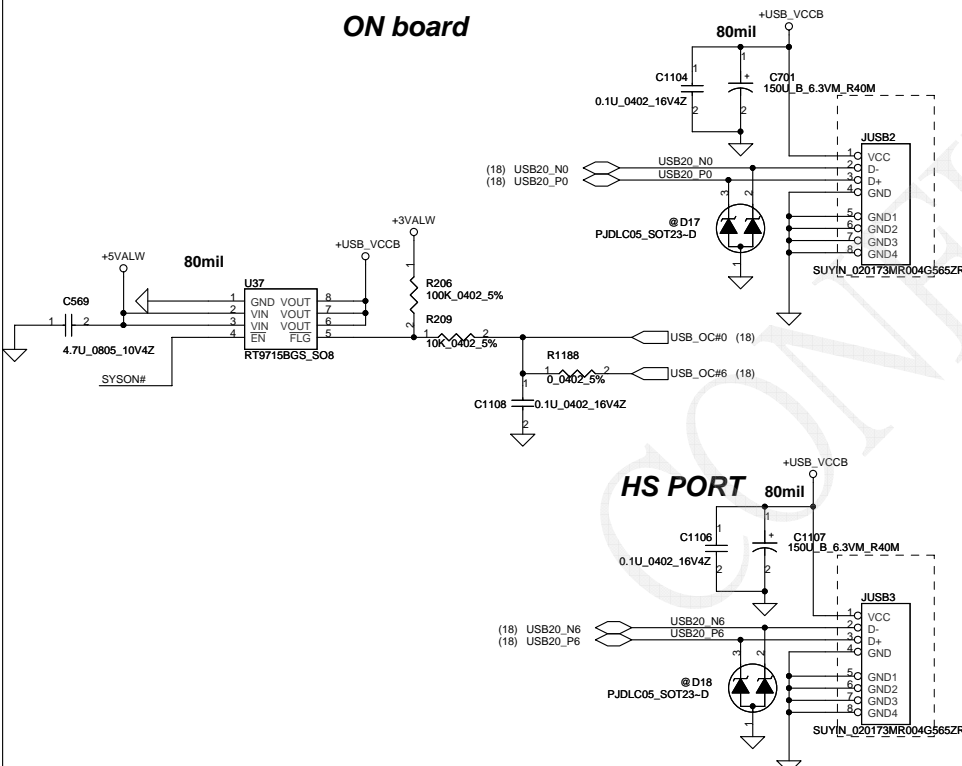
New Card Power Switch



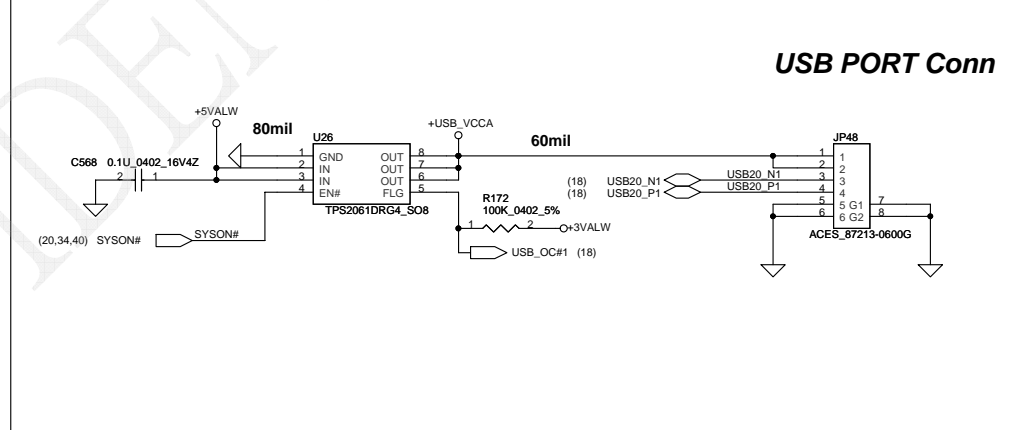
New Card Socket (Left/TOP)



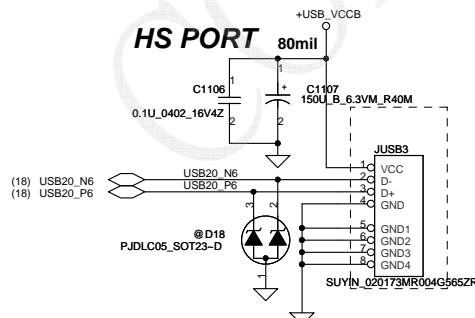
ON board



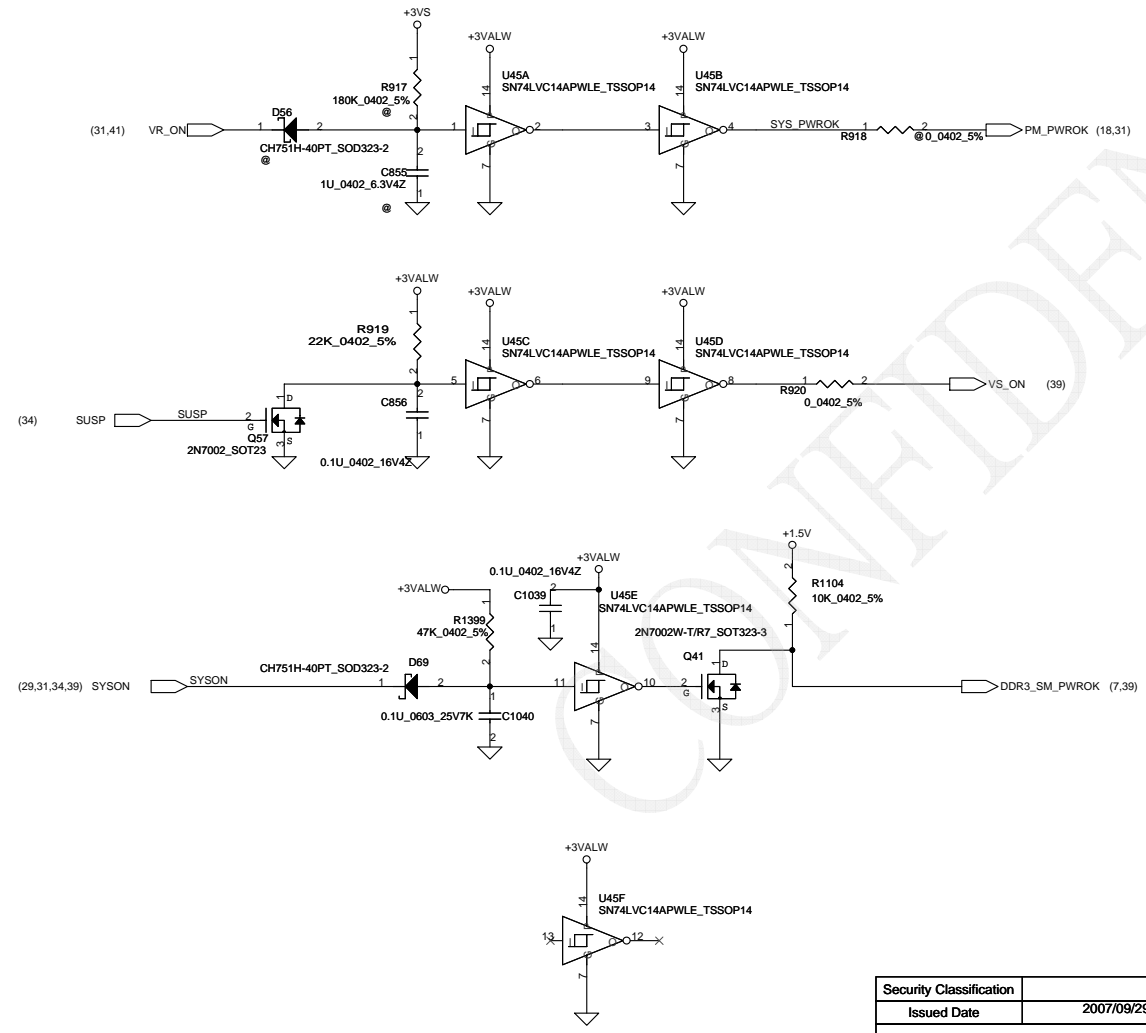
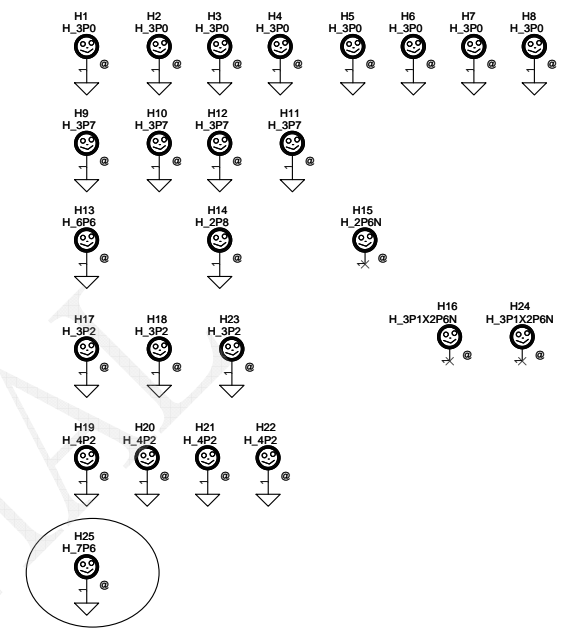
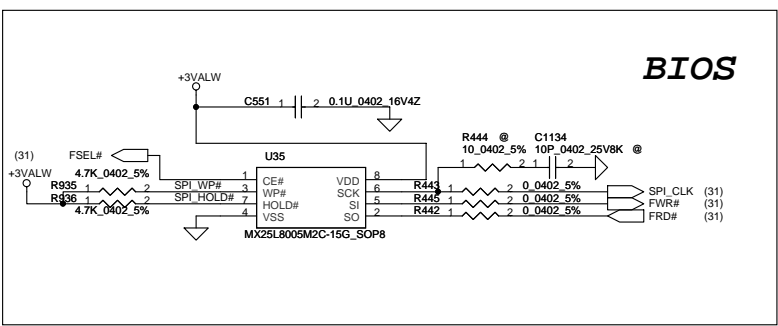
USB PORT Conn



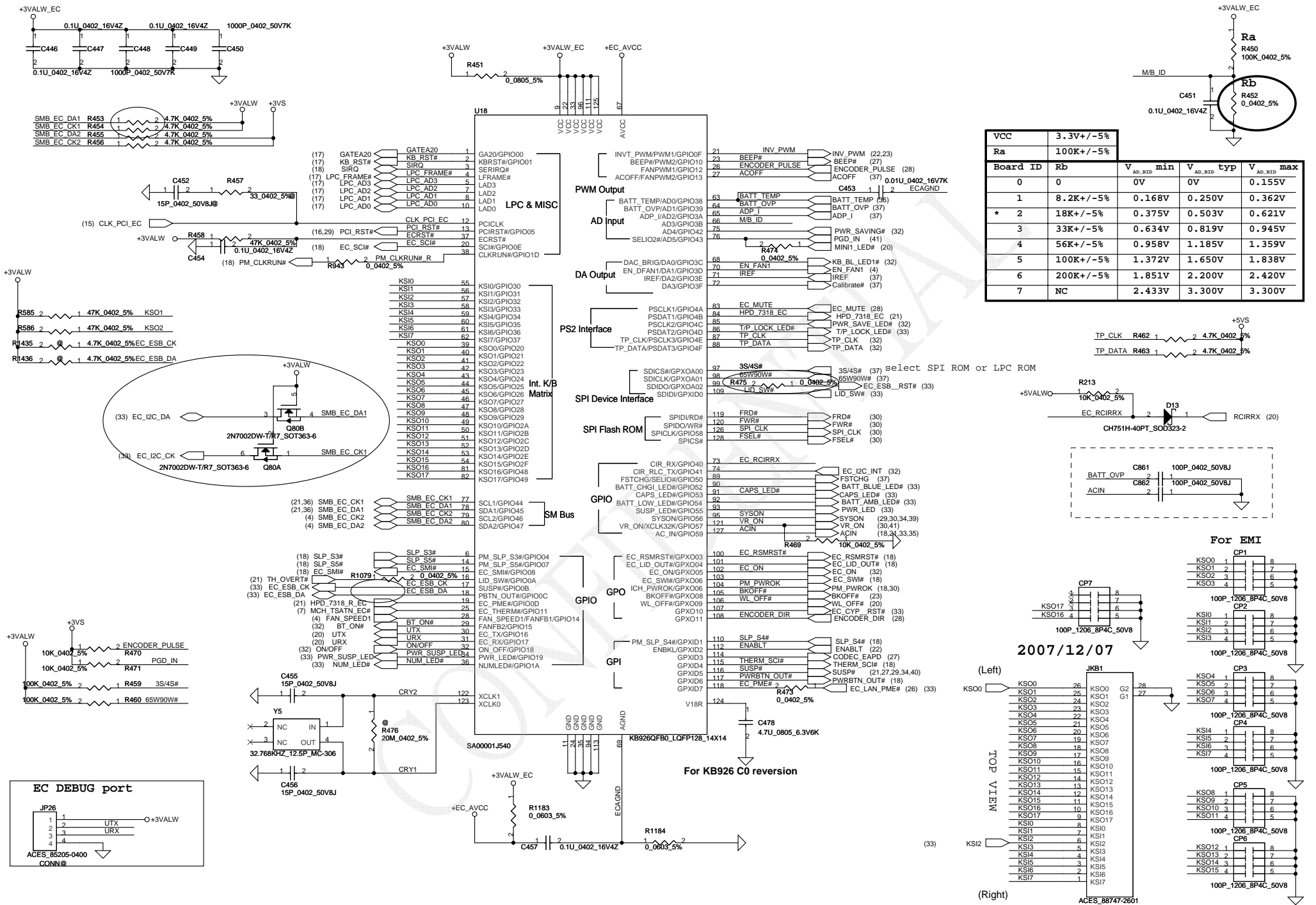
HS PORT



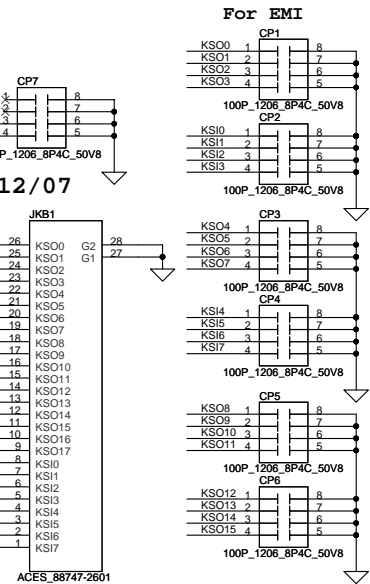
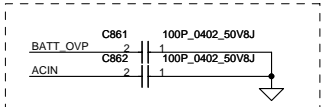
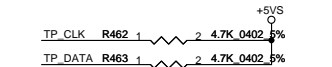
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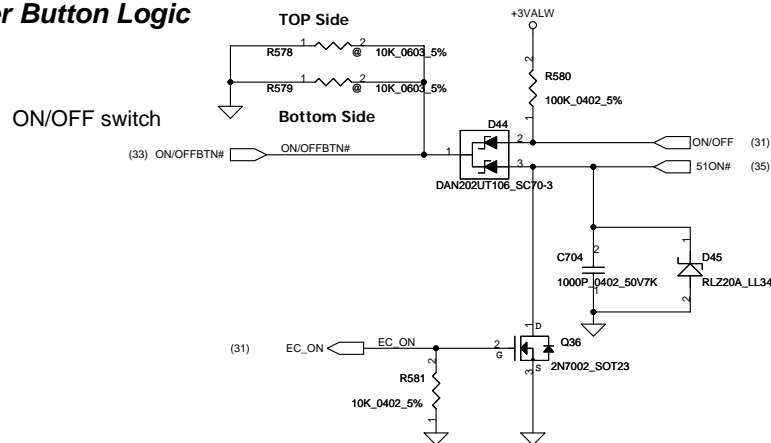
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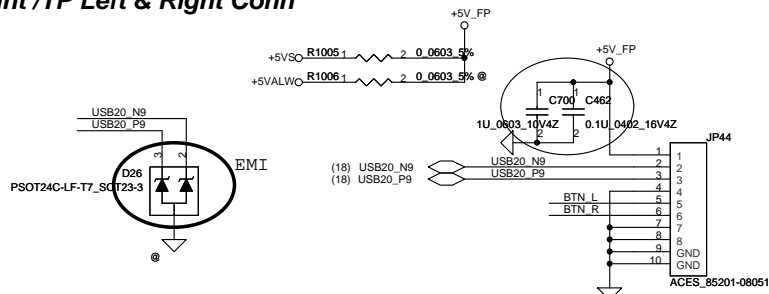
VCC	3.3V+/-5%			
Ra	100K+/-5%			
Board ID	Rb	V _{AD_RID} min	V _{AD_RID} typ	V _{AD_RID} max
0	0	0V	0V	0.155V
1	8.2K+/-5%	0.168V	0.250V	0.362V
* 2	18K+/-5%	0.375V	0.503V	0.621V
3	33K+/-5%	0.634V	0.819V	0.945V
4	56K+/-5%	0.958V	1.185V	1.359V
5	100K+/-5%	1.372V	1.650V	1.838V
6	200K+/-5%	1.851V	2.200V	2.420V
7	NC	2.433V	3.300V	3.300V



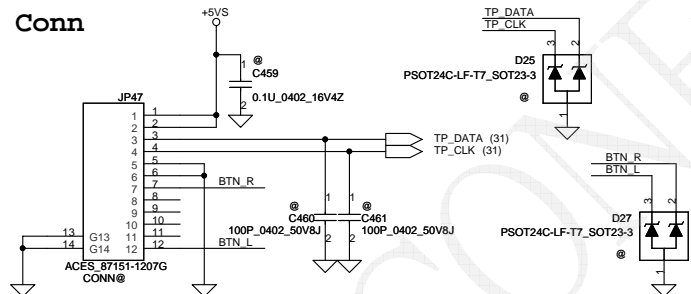
Power Button Logic



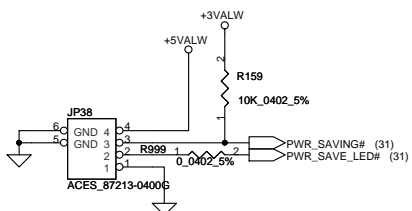
Finger Print /TP Left & Right Conn



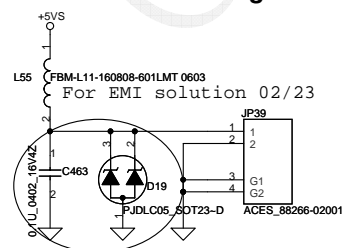
T/P Board Conn



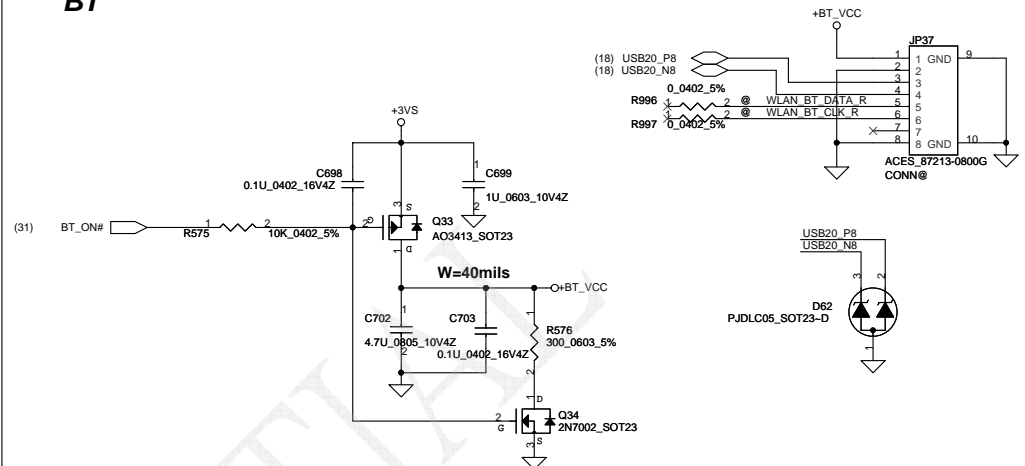
POWER SAVING Conn



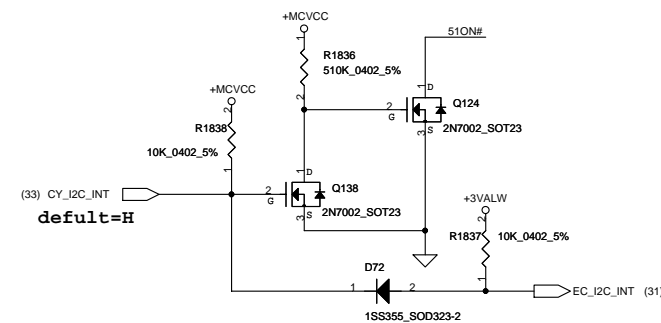
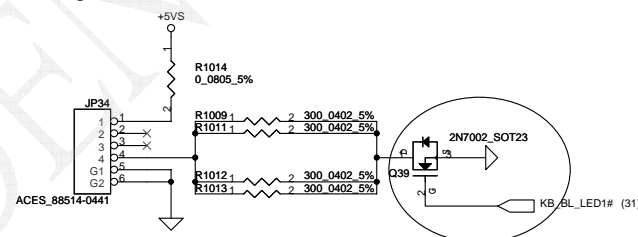
ACER LOGO BackLight Conn



BT

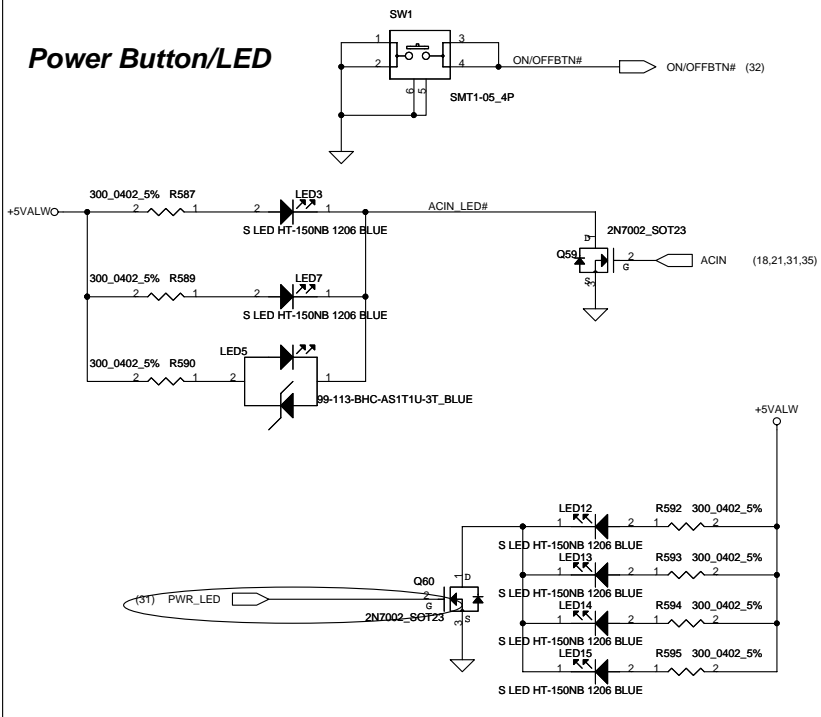


KB back light Conn

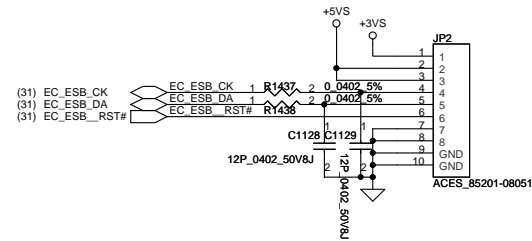


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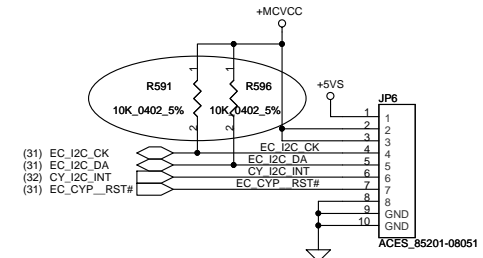
Power Button/LED



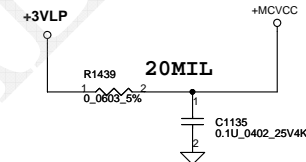
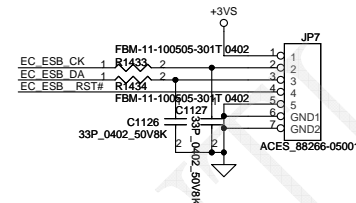
CAP Sensor left(ENE)



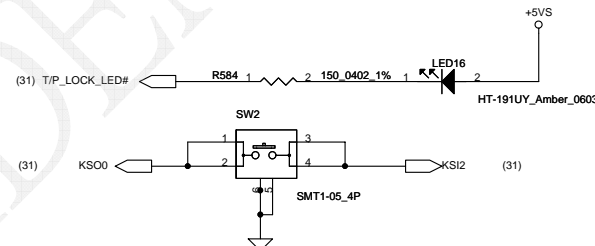
CAP Sensor right(Cypress)



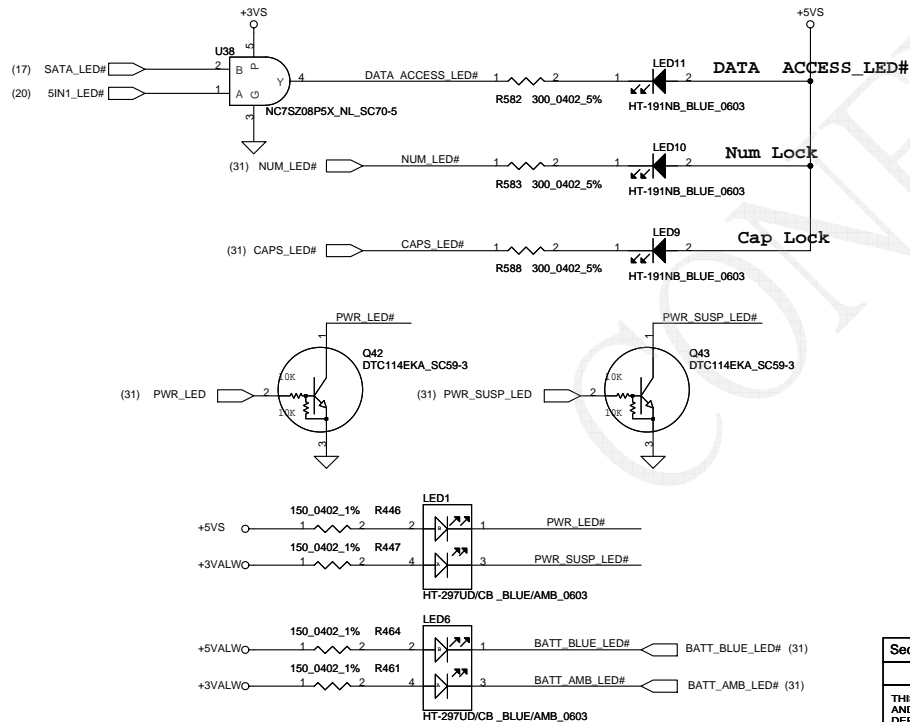
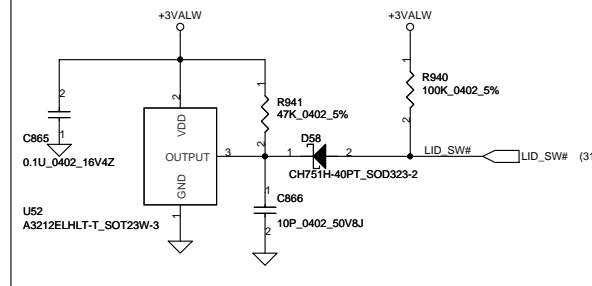
CAP Sensor B COVER(ENE)



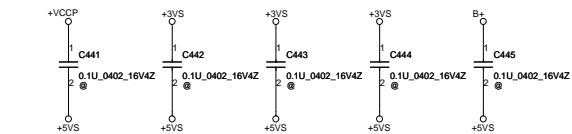
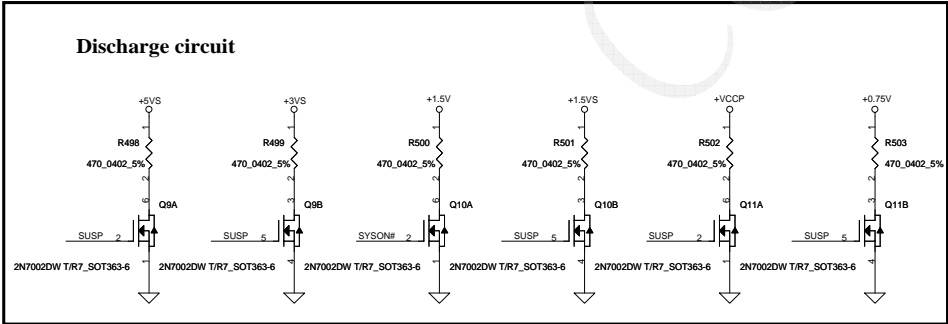
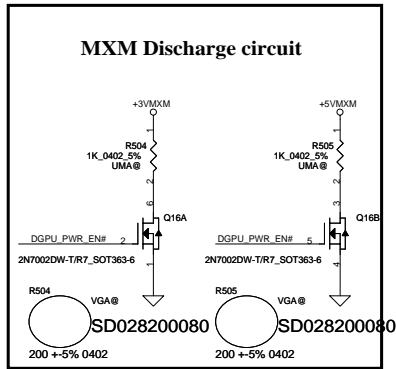
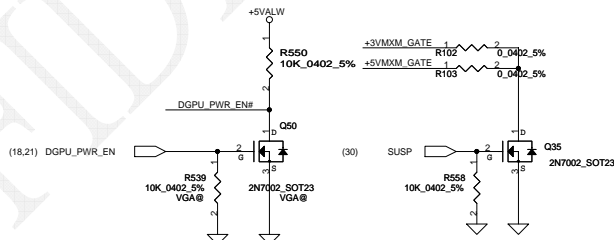
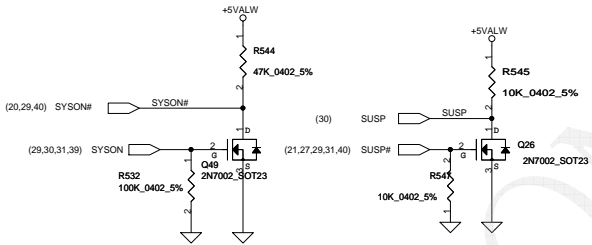
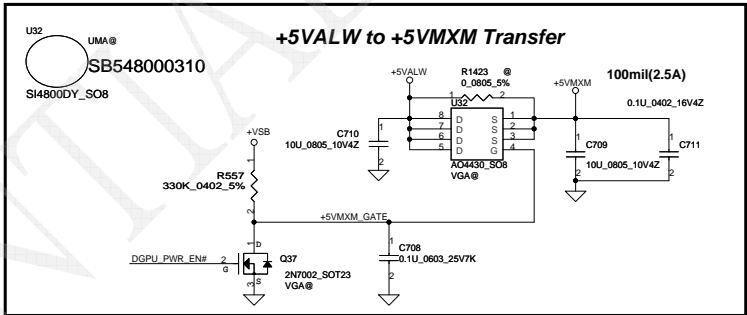
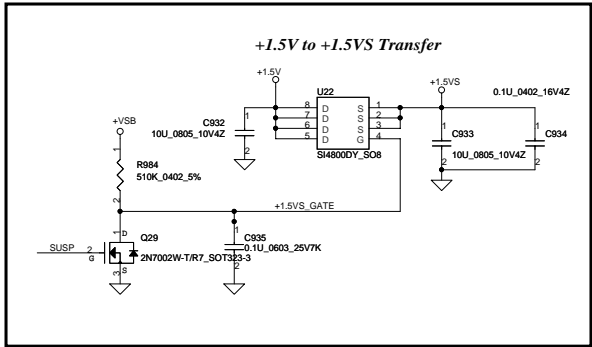
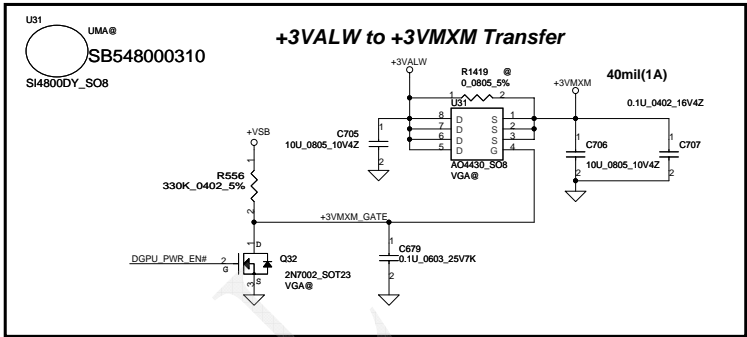
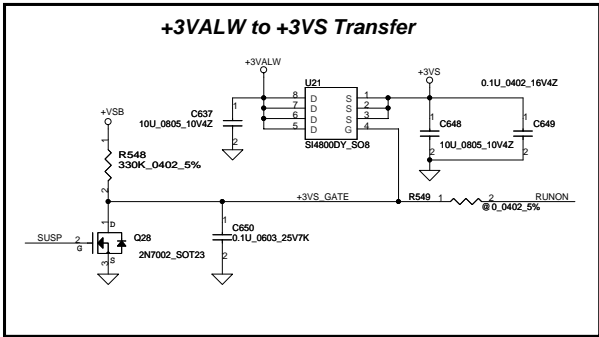
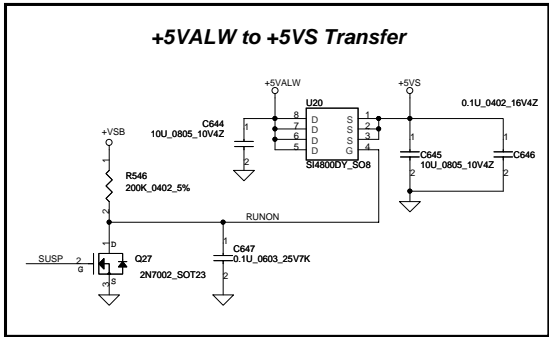
T/P Lock Button/LED



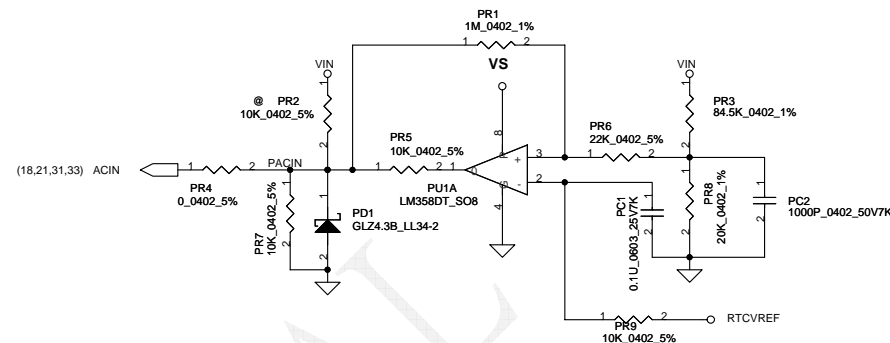
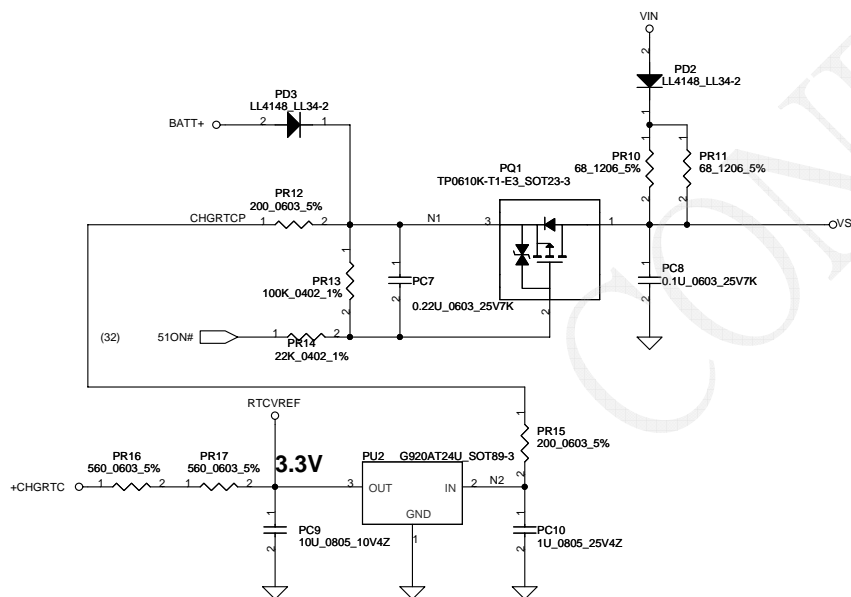
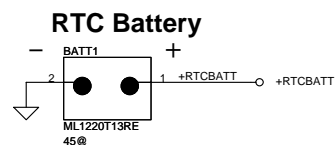
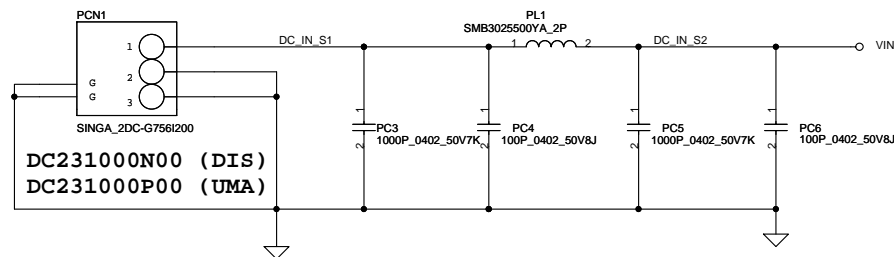
(Hall Effect Switch)



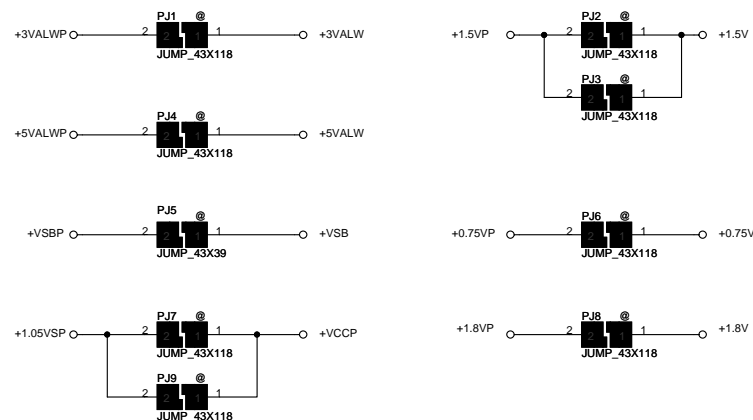
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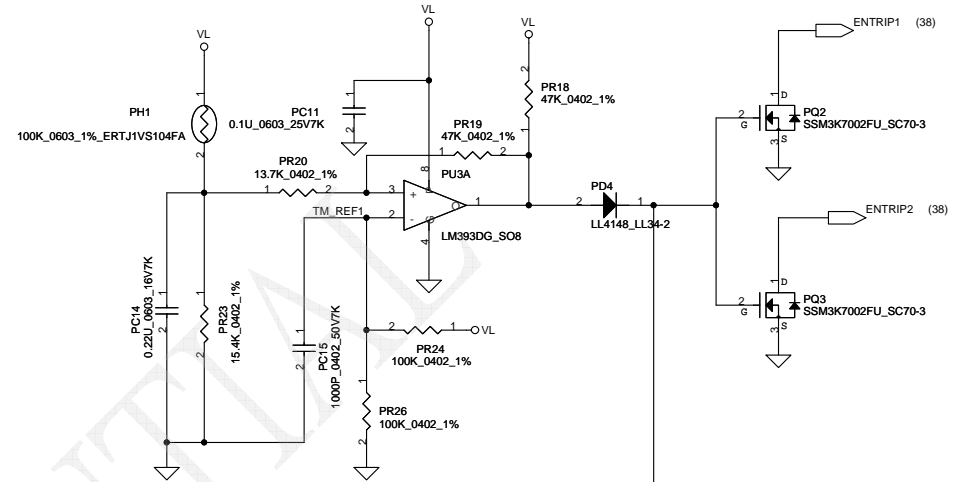


	Min.	Typ	Max.
H-->L	17.208V	17.212V	17.217V
L-->H	17.879V	17.894V	17.909V

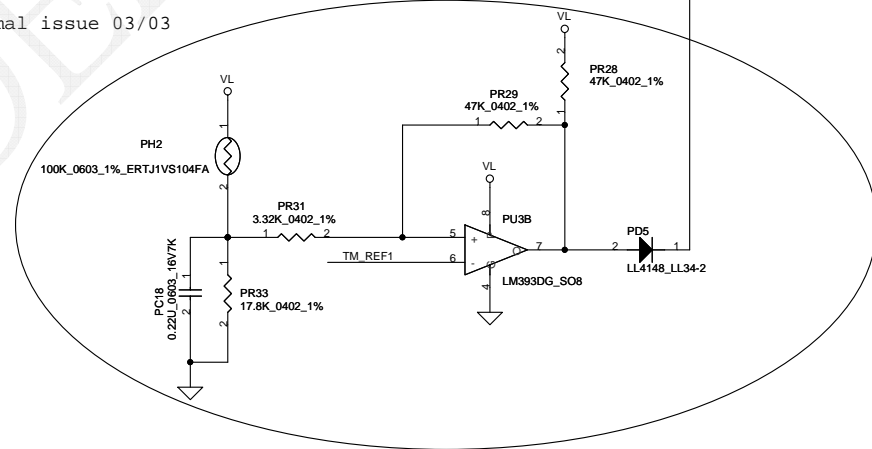


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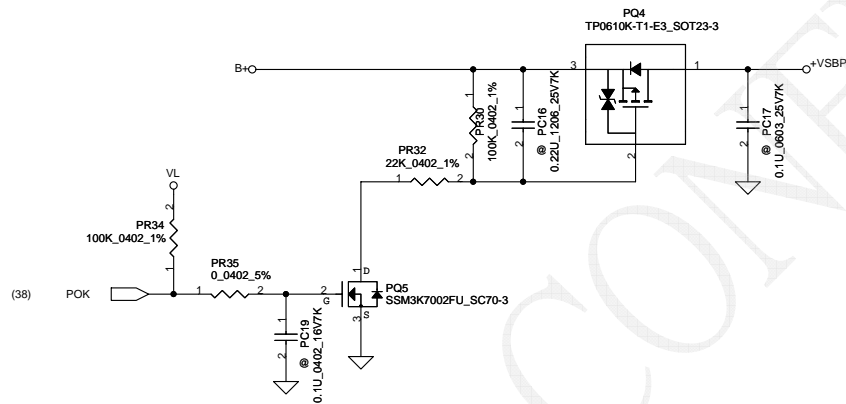
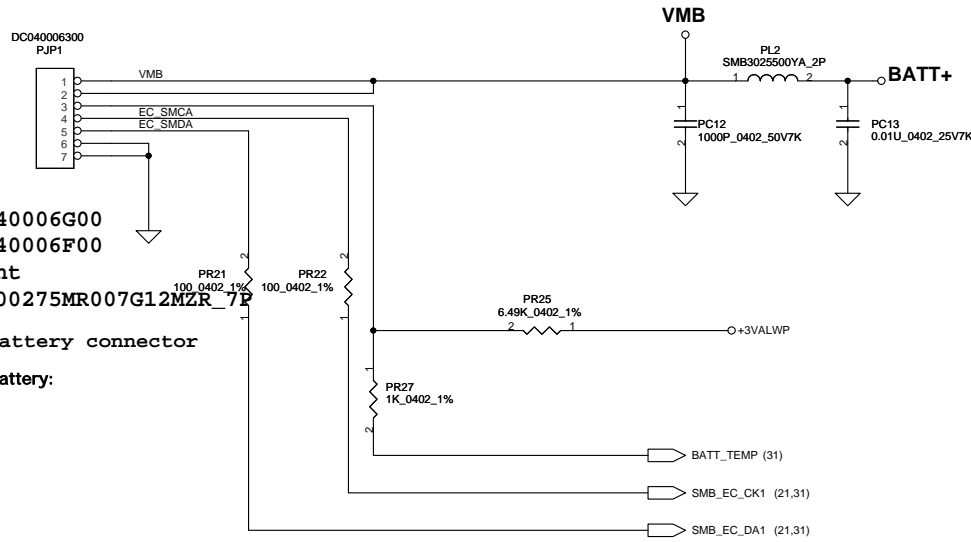
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



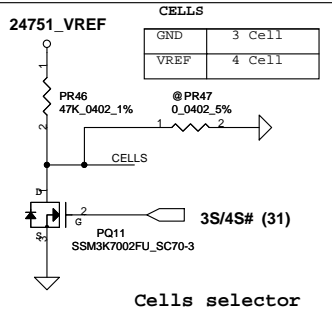
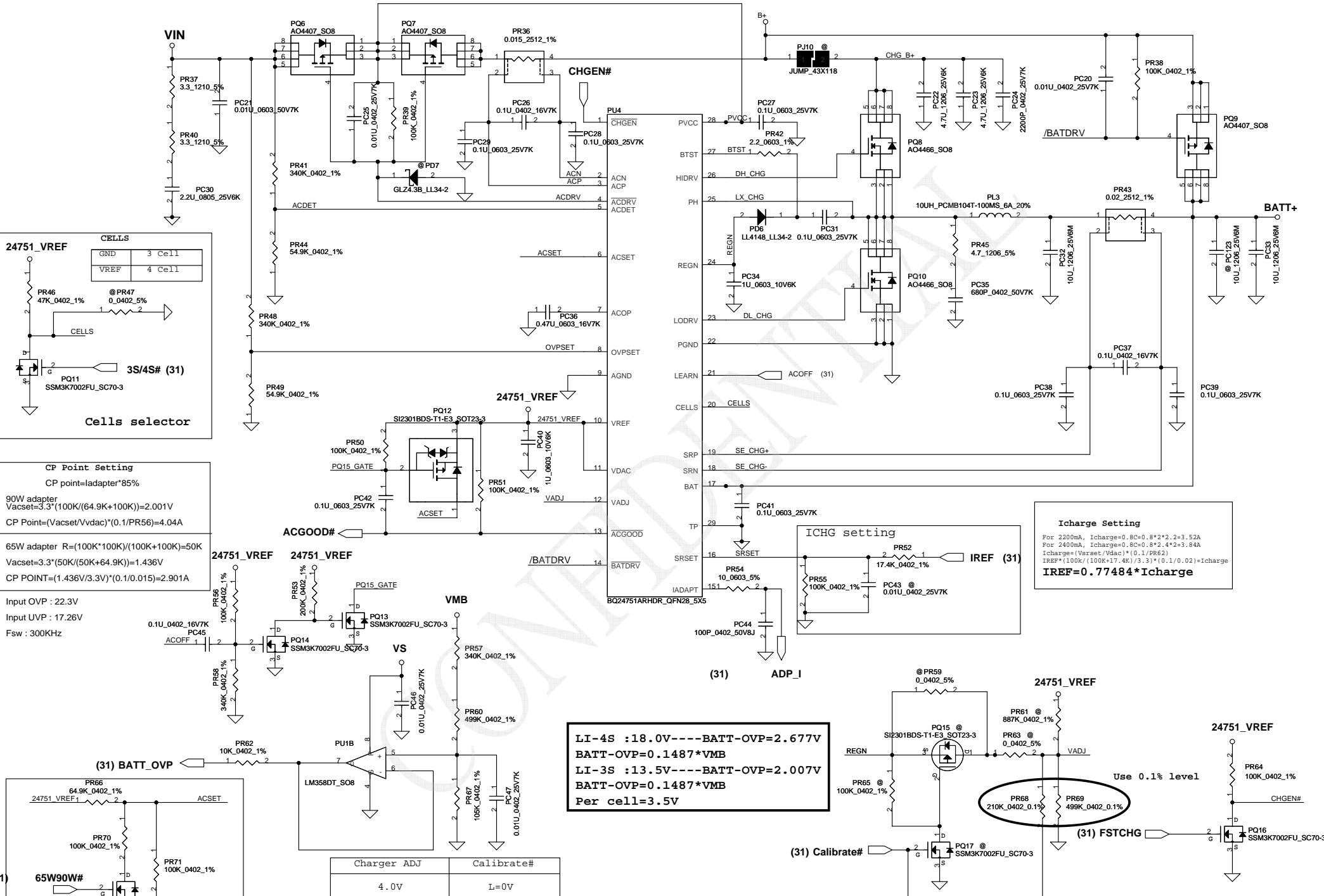
PH2 near main Battery CONN :
BAT. thermal protection at 76 degree C
Recovery at 72 degree C



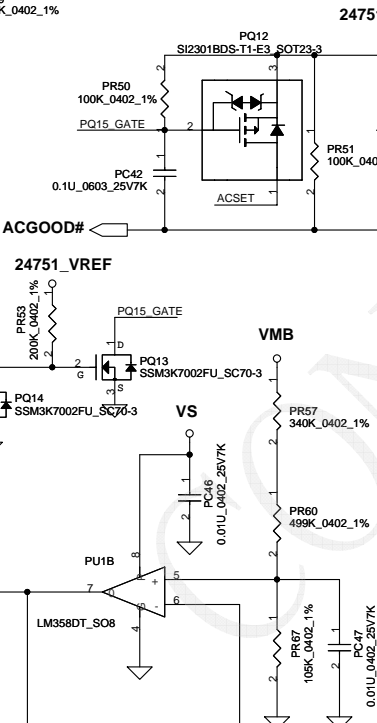
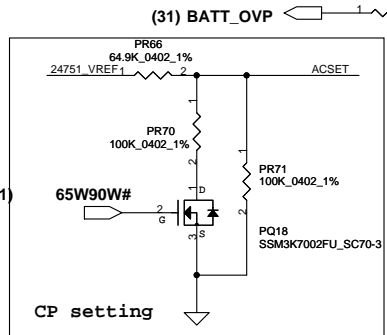
solve battery thermal issue 03/03



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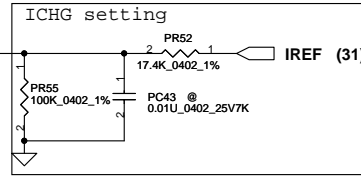


CP Point Setting
CP point=ladder*85%
90W adapter
 $V_{acset}=3.3 \cdot (100K/(64.9K+100K))=2.001V$
CP Point=(V_{acset}/V_{vdac})*(0.1/PR56)=4.04A
65W adapter $R=(100K \cdot 100K)/(100K+100K)=50K$
 $V_{acset}=3.3 \cdot (50K/(50K+64.9K))=1.436V$
CP POINT=($1.436V/3.3V$)*(0.1/0.015)=2.901A
Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz

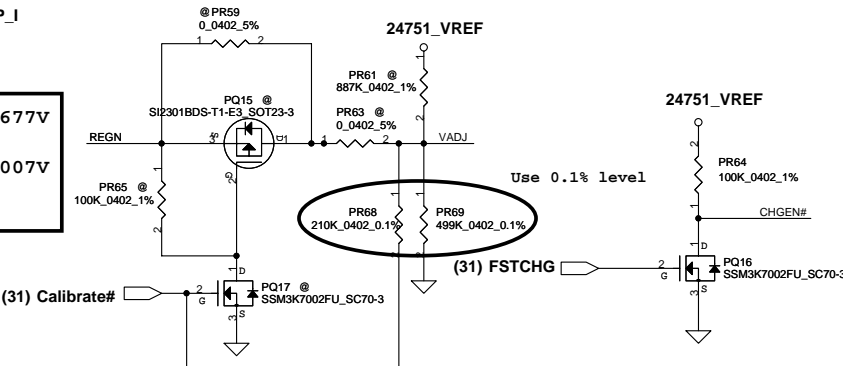


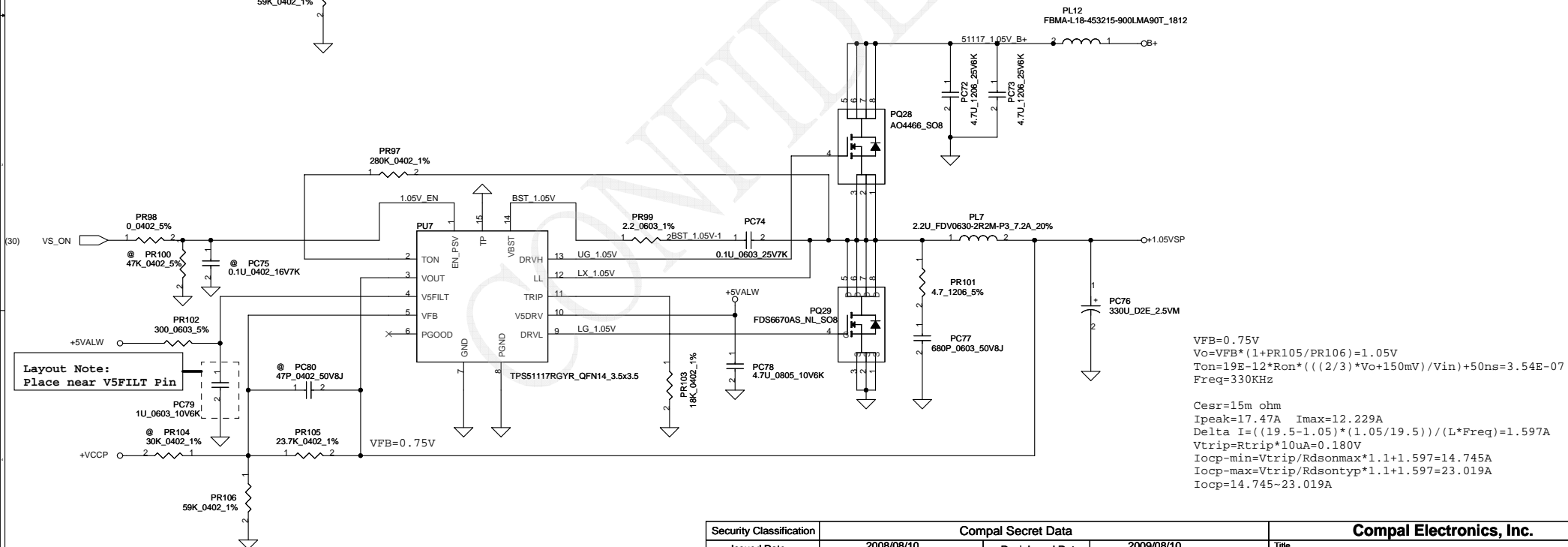
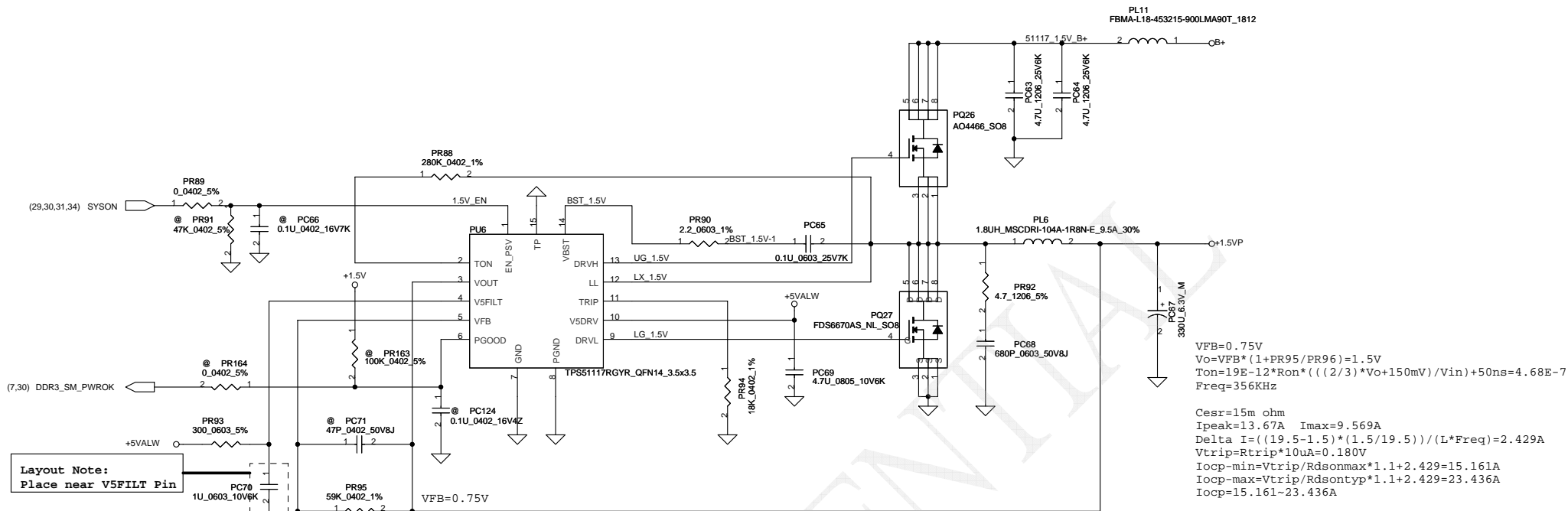
Charger ADJ	Calibrate#
4.0V	L=0V
4.2V	1.8755V
4.3V	2.8132V
4.35V	H=3.3V

LI-4S :18.0V----BATT-OVP=2.677V
BATT-OVP=0.1487*VMB
LI-3S :13.5V----BATT-OVP=2.007V
BATT-OVP=0.1487*VMB
Per cell=3.5V

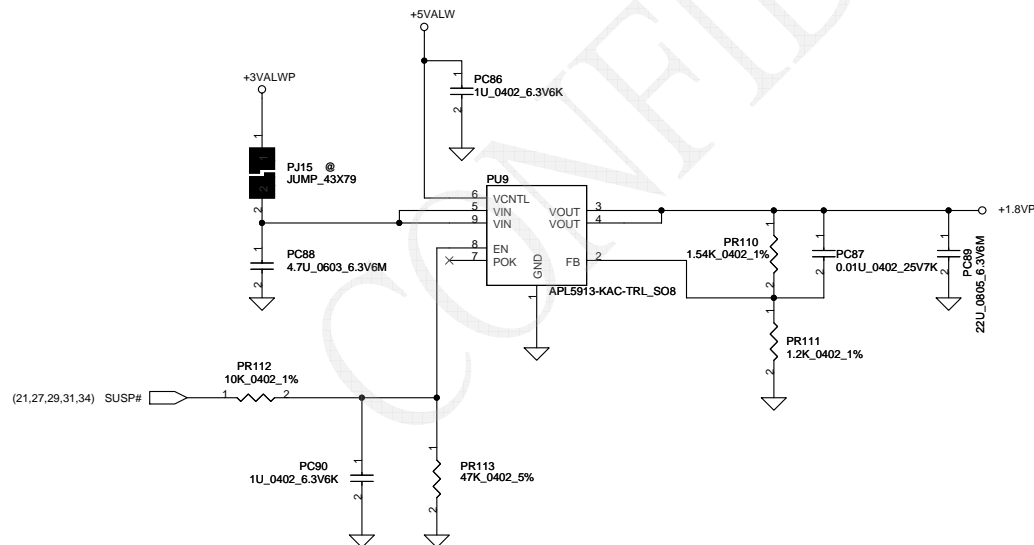
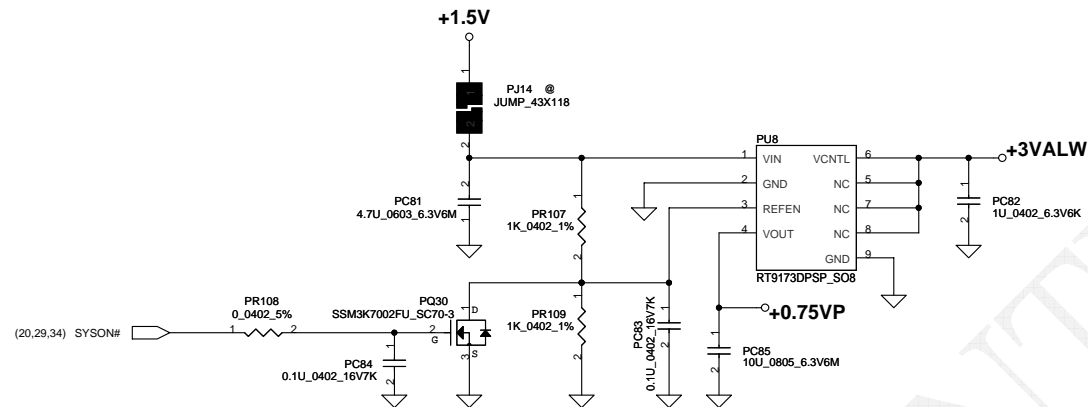


Icharge Setting
For 2200mA, Icharge=0.8C*0.8*2.2=3.52A
For 2400mA, Icharge=0.8C*0.8*2.4=3.84A
Icharge=(Vset/Vdac)*(0.1/PR62)
IREF*(100K/(100K+17.4K)/3.3)*(0.1/0.02)=Icharge
IREF=0.77484*Icharge

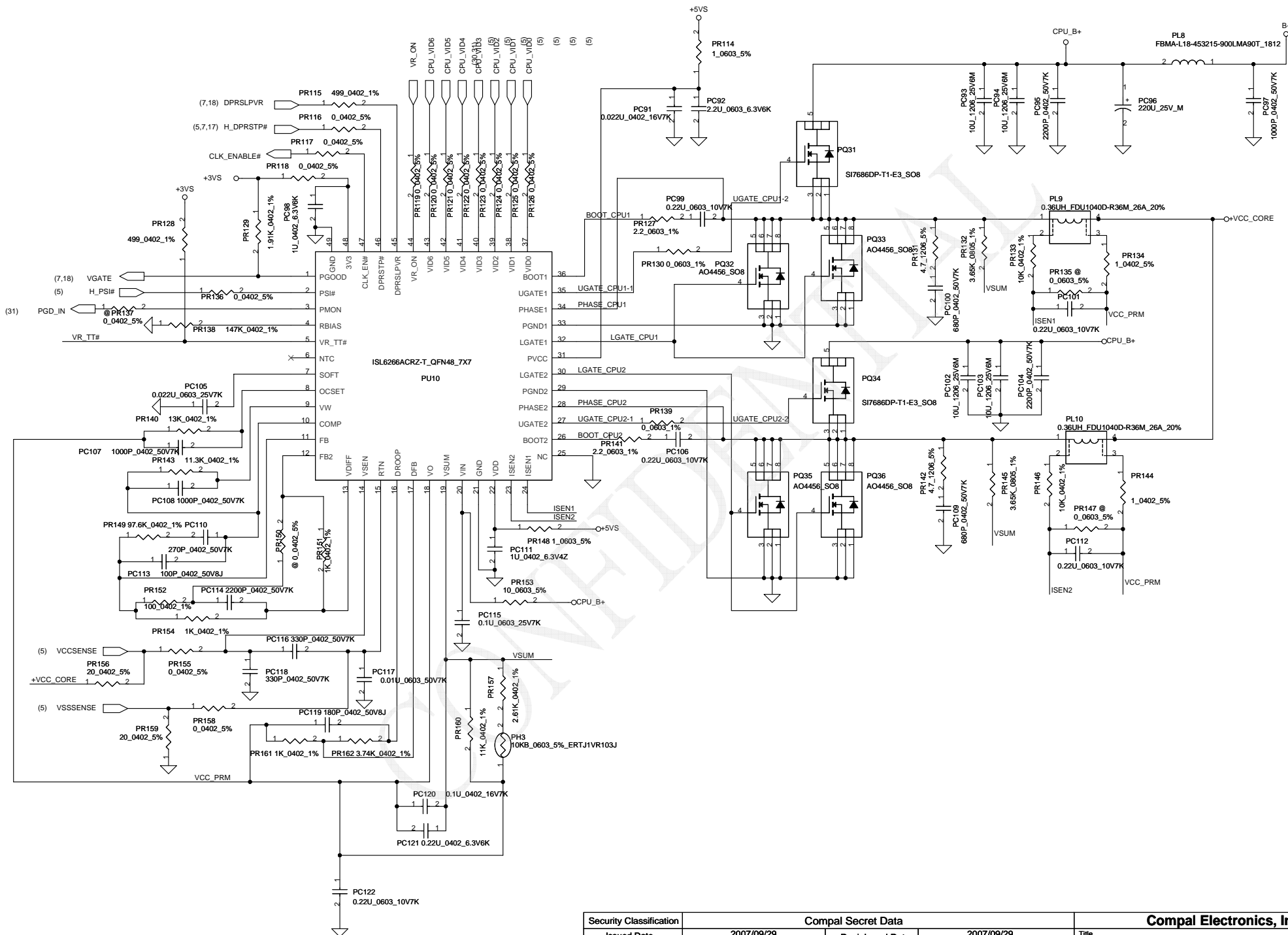




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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Unite parts			PQ5,PQ11,PQ13,PQ14,PQ16,PQ17,PQ18,PQ30 Change from SB000006800、SB000009080 to SB000009610	2008 12/19	EVT
2		EMI request			Add PR80,PR81,PR131,PR142 SD001470B80 (S RES 1/4W 4.7 +-5% 1206)	2008 12/19	EVT
3		EMI request			Change PR78,PR79,PR127,PR141 from 0 to 2.2 (SD014220B80)	2008 12/19	EVT
4		Reduse 1.5V, 1.05V frequency to about 300KHz			Change PR88,PR97 from 180K to 280K(SD034280380)	2008 12/19	EVT
5	Output voltage error	Set 1.8V voltage			Change PR111 from 1.71K to 1.2K(SD034120180)	2008 12/19	EVT
6		Down size			Change PC88 from 0805 to 0603(SE093475K80)	2008 12/19	EVT
7	Heavy load efficiency fail	Raise heavy load efficiency		38	Change PL4,PL5 from 10uF to 4.7uF(SH000006J80)	2008 12/19	EVT
8		EMI request			Add PC58,PC59 S CER CAP 680P 50V K X7R 0603 (SE025681K80)	2008 12/19	EVT
9		EMI request			Add PC100,PC109 S CER CAP 680P 50V K X7R 0402 (SE074681K80)	2008 12/19	EVT
10				41	Change PR143 from 8.25K to 11.3K(SD034113280)	2008 12/19	EVT
11		Improve load line		41	Change PR162 from 4.42K to 3.74K(SD034374180)	2008 12/22	EVT
12		New charge voltage setting		37	Delete PQ15,PQ17,PR61,PR63,PR65	2008 12/23	EVT
13		New charge voltage setting		37	Add PR68 210K_0402_1%(SD034210380)	2008 12/23	EVT
14		New charge voltage setting		37	Change PR69 from 221K to 49.9K(SD034499280)	2008 12/23	EVT
15	Battery can't charge to 100%			37	Change PR69 from 49.9K to 499K(SD034499380)	2009 01/12	DVT
16	HDMI 5V voltage test fail(should 4.8~5.3V)	Raise 5V voltage		38	Change PR75 from 20K to 19.1K(SD034191280)	2009 01/17	DVT
17		Prevent spike		37	Add PD7	2009 01/21	DVT
18		Improve charge voltage		37	Change PR68, PR69 from 1% to 0.1%	2009 01/22	DVT
19		EMI request		39	Change PR90, PR99 from 0 to 2.2(SD014220B80) Enable PR92, PR101, PC68, PC77	2009 02/04	DVT
20		EMI request		39	Change PJ12 to PL11(SM010020720) Change PJ13 to PL12(SM010020720)	2009 02/04	DVT
21		EMI request		37	Change PR42 from 0 to 2.2(SD014220B80) Enable PR45, PC35	2009 02/04	DVT
22	Protect logic low	Set trigger point at 76		36	Enable PD5, PH2, PR28, PR29, PR31, PR33, PC18	2009 02/25	PVT
23							

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